

# MS-7676

UATX Ver:2.1

## CPU:

INTEL - Sandy Bridge LGA 1155

## System Chipset:

INTEL - Cougar Point PCH

## OnBoard Chipset:

Clock Gen:IDT 4105

HD Audio Codec:RTL892

LAN:RTL 8111E 10/100/1000

SIO:FIN71889AD

Flash ROM: 64 Mb SPI (PCH)\* 2

## Main Memory:

DDR3 (1066/1333MHz) \* 4 (Dual Channel)

## Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X4) Slot \* 1

PCI Express (X1) Slot \* 2

## PWM:

Controller:VRD12 UPI6234 (6+2-Phase )Dr.MOS

CPU+GPU

Controller:uP6113 Dr.MOS

CPU VTT CPU SA

Controller:uP6103A

DDR PCH

## ACPI:

UPI

## Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

USB2.0 RearX4 Front x8(PCH)

USB3.0 RearX2 (NEC uPD720200)

1394 Controller - VT6315N-CE

D-SUB \*1

DVI-D PORT\*1

HDMI \*1

TPM Header \*1

COM Header \*1

on BOARD BUZZER

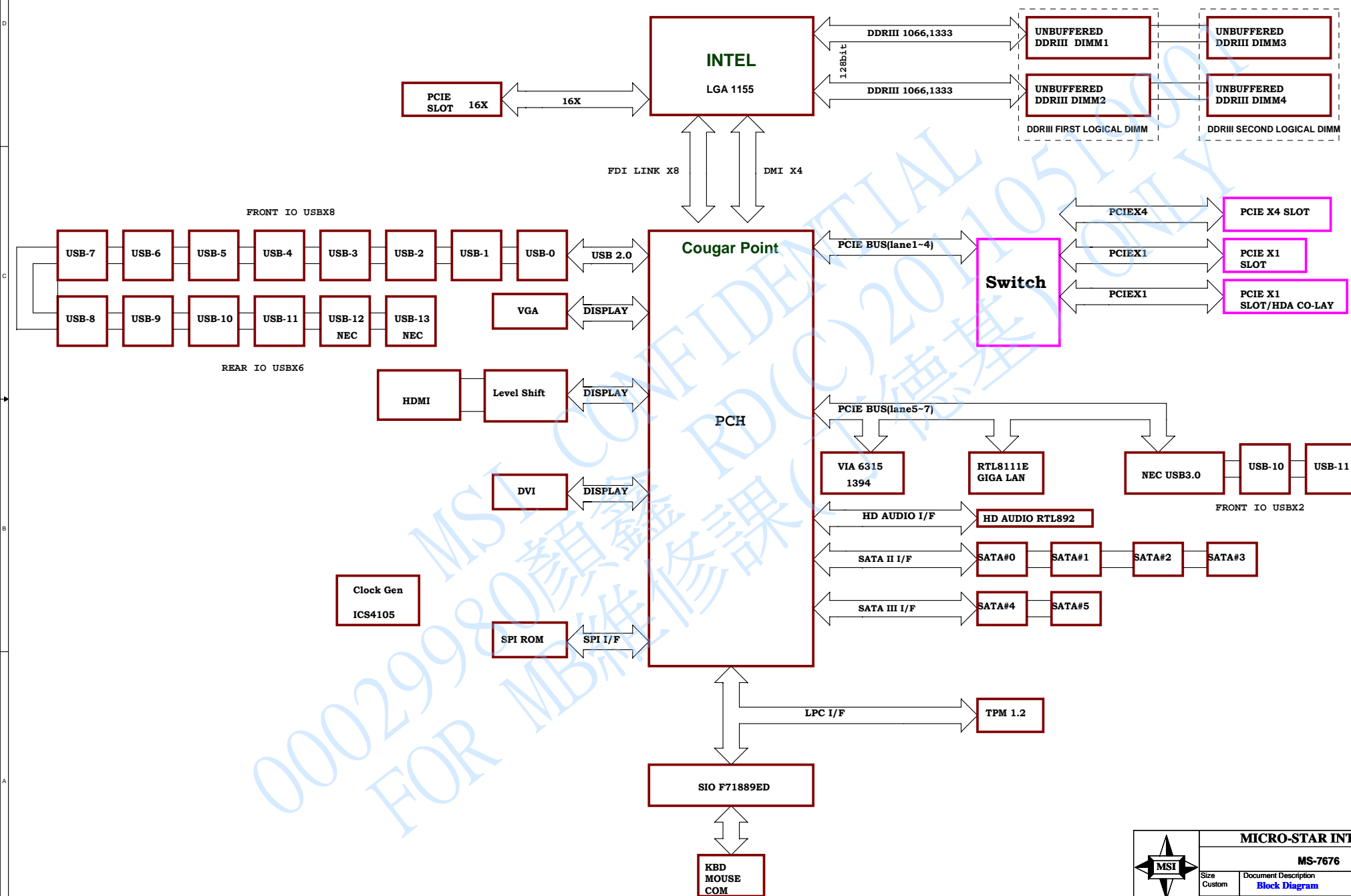
Title	Page
Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG	3
CPU-Memory	4
CPU-Power	5
CPU-GND	6
DDR III DIMM 1 / DIMM 2	7
DDR III DIMM 3 / DIMM 4	8
CLK GEN4106	9
CP-PCI/E/DMI/USB/CLK	10
CP-SATA/HOST/FAN/GPIO/VGA	11
CP-SMB/LPC/AUDIO/RTC	12
CP-POWER	13
CP-GND/NVRAM	14
CP Strap	15
PCIe x16 /x1 /x1HDA CO-LAY	16
PCIEx4 Slots	17
SIO-Fintek F71889AD(EUP)	18
MARVELL SATA 6G	19
NEC USB3.0	20
NEC USB3.0 POWER & CONNECT	21
1394 Controller - VT6315N-CE	22
LAN - RTL8111E	23
ALC892_COLAY_ALC887VD	24
DVI transfer	25
HDMI	26
VGA	27
SATA / FAN Control	28
USB Charger	29
USB Connector	30
ACPI Controller UPI	31
Power Saving circuit	32
DDR Power - uP6103 1-Phase	33
PCH Power - uP6103 1-Phase	34
CPU_VTT - uP6113- 1-Phase	35
CPU_SA - uP6113 1-Phase	36
VRD12 - UPI6234 6+2-Phase	37
UP6234 6-Phase CPU(Dr.Mos)	38
UP6234 2-Phase GPU(Dr.Mos)	39
ATX F_Panel/EMI/TPM	40
PHASE Dropping & PSI & LED	41
XDP / Manual Parts	42



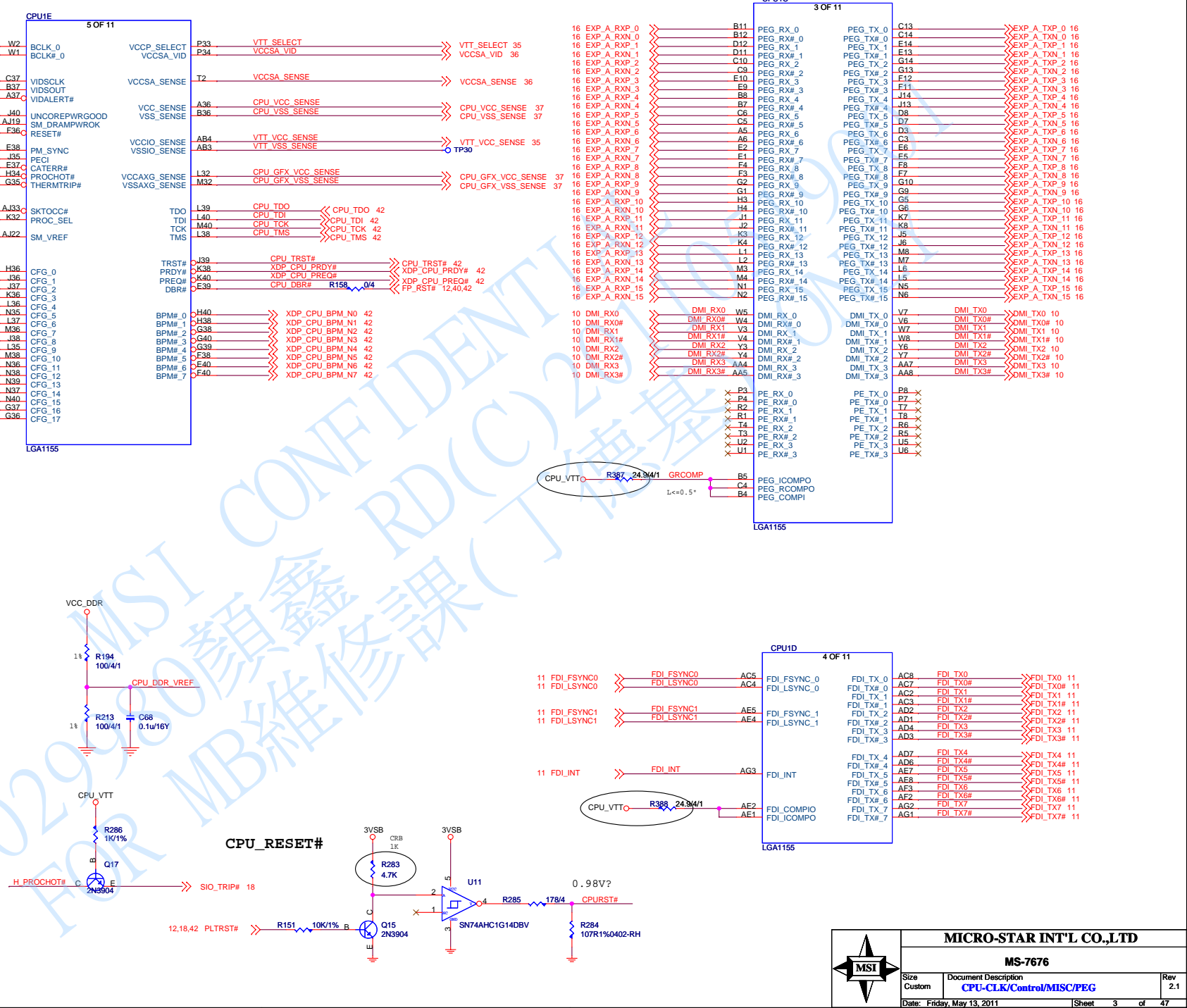
MICRO-STAR INT'L CO.,LTD


MS-7676

Size Custom	Document Description Cover Sheet	Rev 2.1
Date: Friday, May 13, 2011	Sheet 1 of 47	



PEG CONFIG TABLE			
SEL2	SEL1	SEL0	PCIE CONFIG
1	1	1	1 X 16
1	1	0	2 X 8





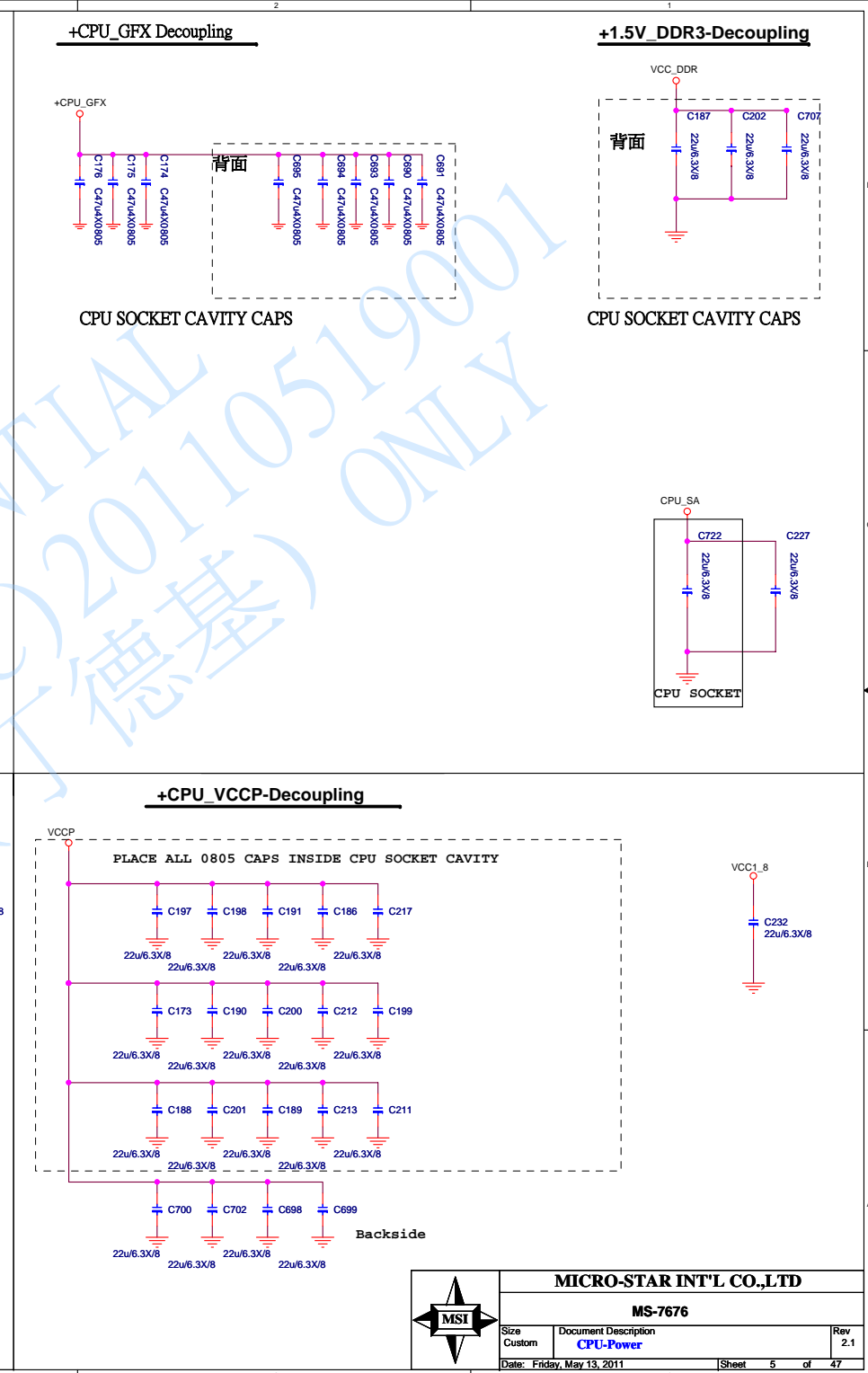
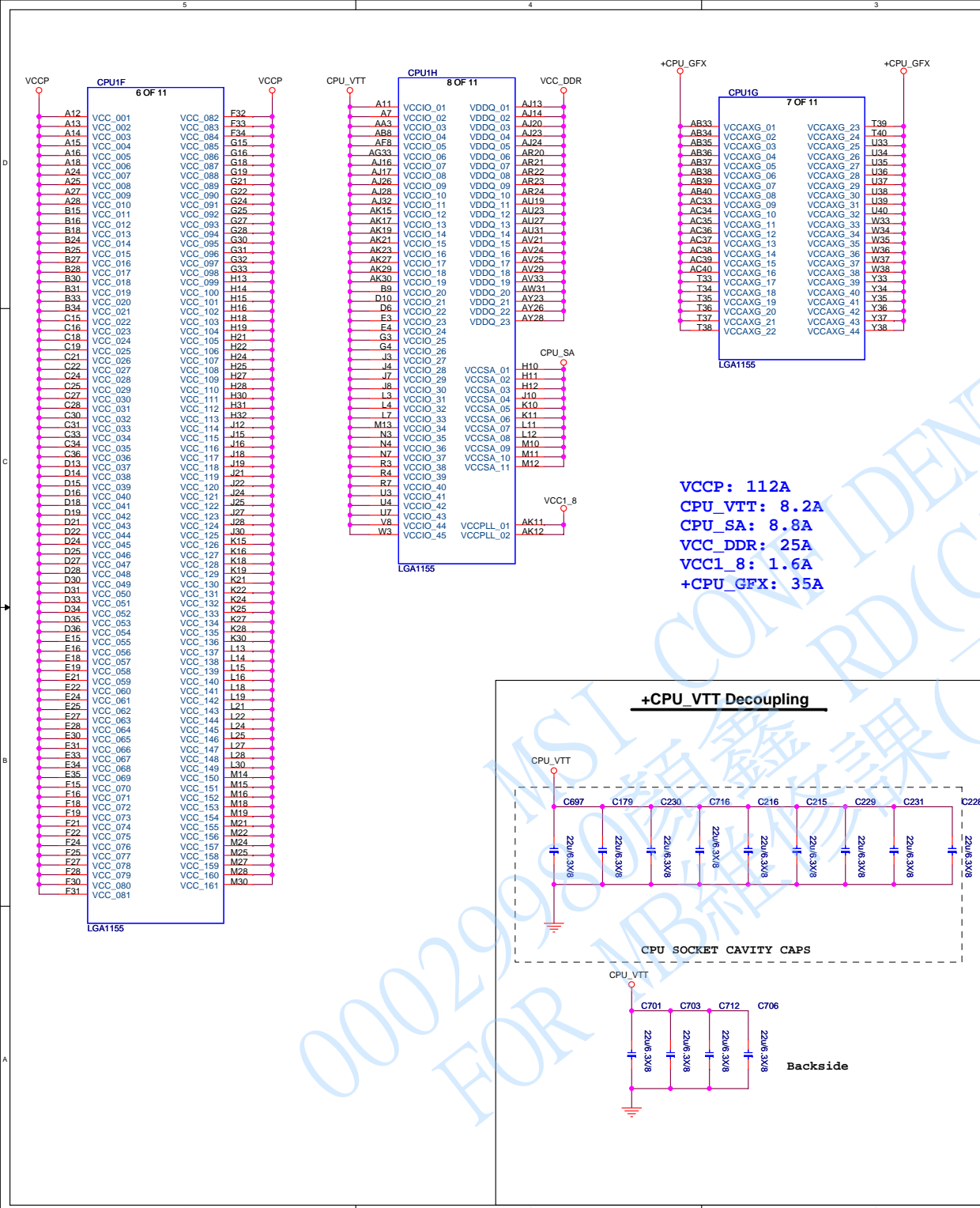
**MICRO-STAR INT'L CO.,LTD**

**MS-7676**

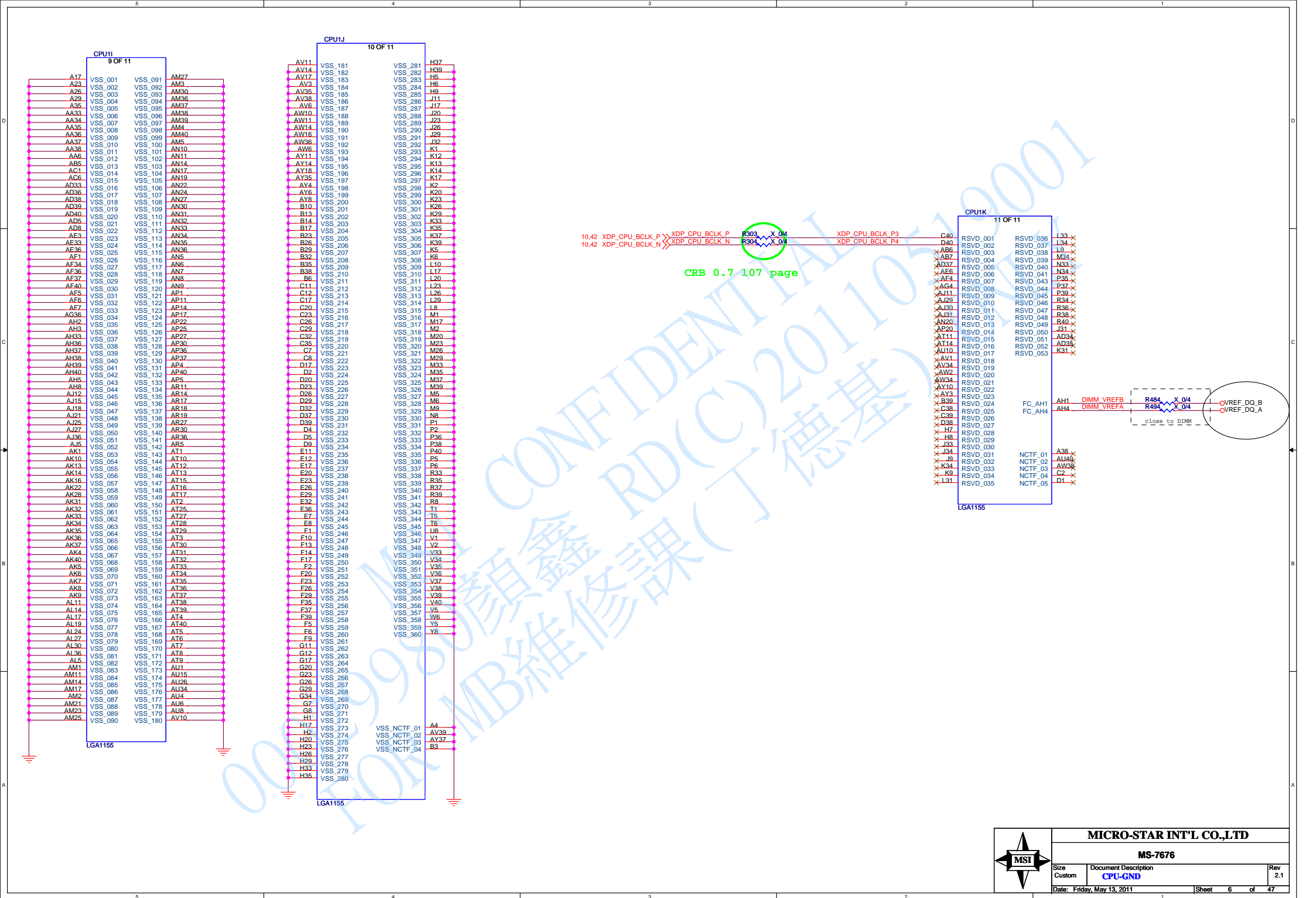
Size: Custom    Document Description: CPU-CLK/Control/MISC/PEG    Rev: 2.1

Date: Friday, May 13, 2011    Sheet: 3 of 47







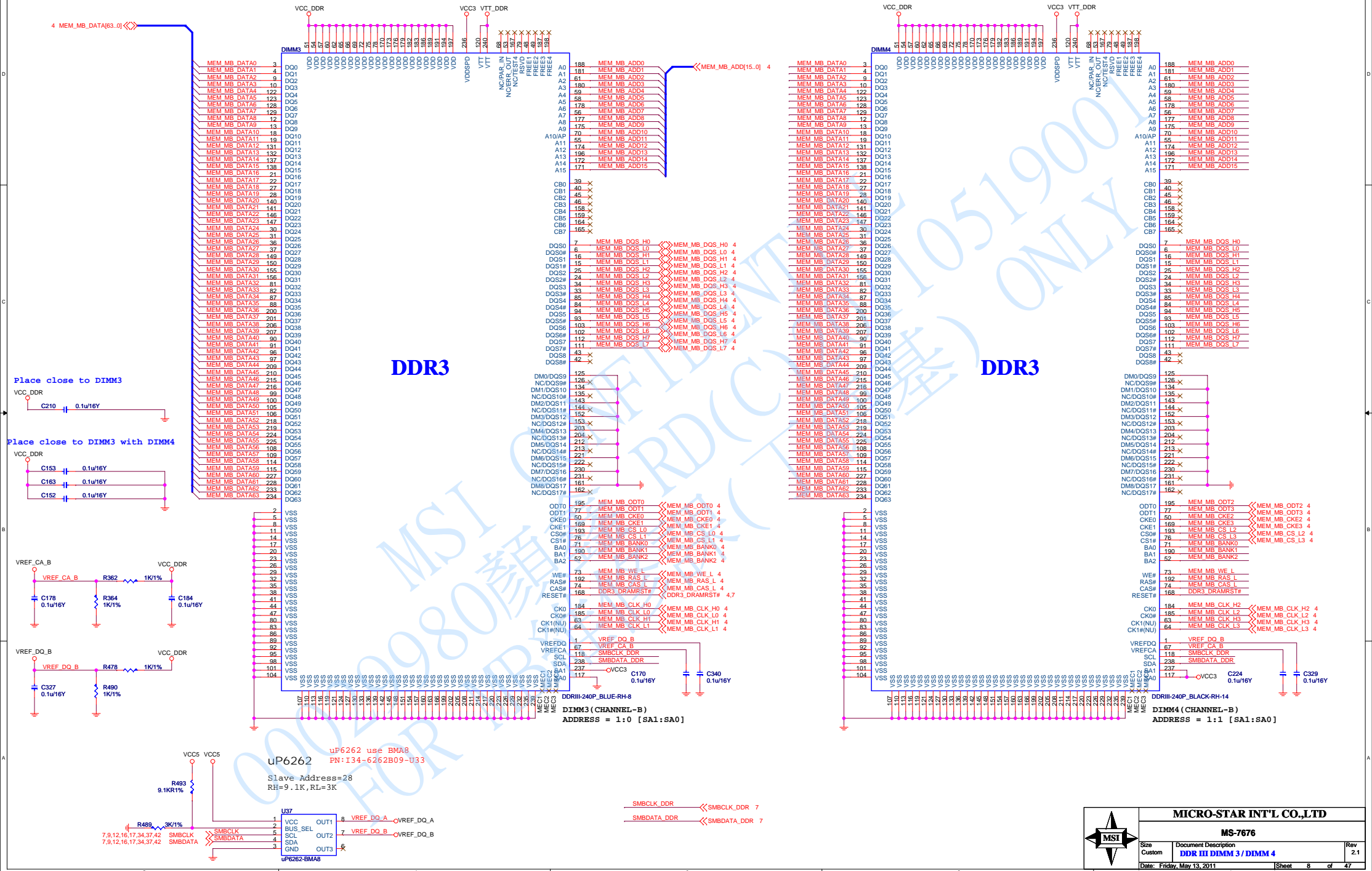


## DDRIII DIMM\_A1

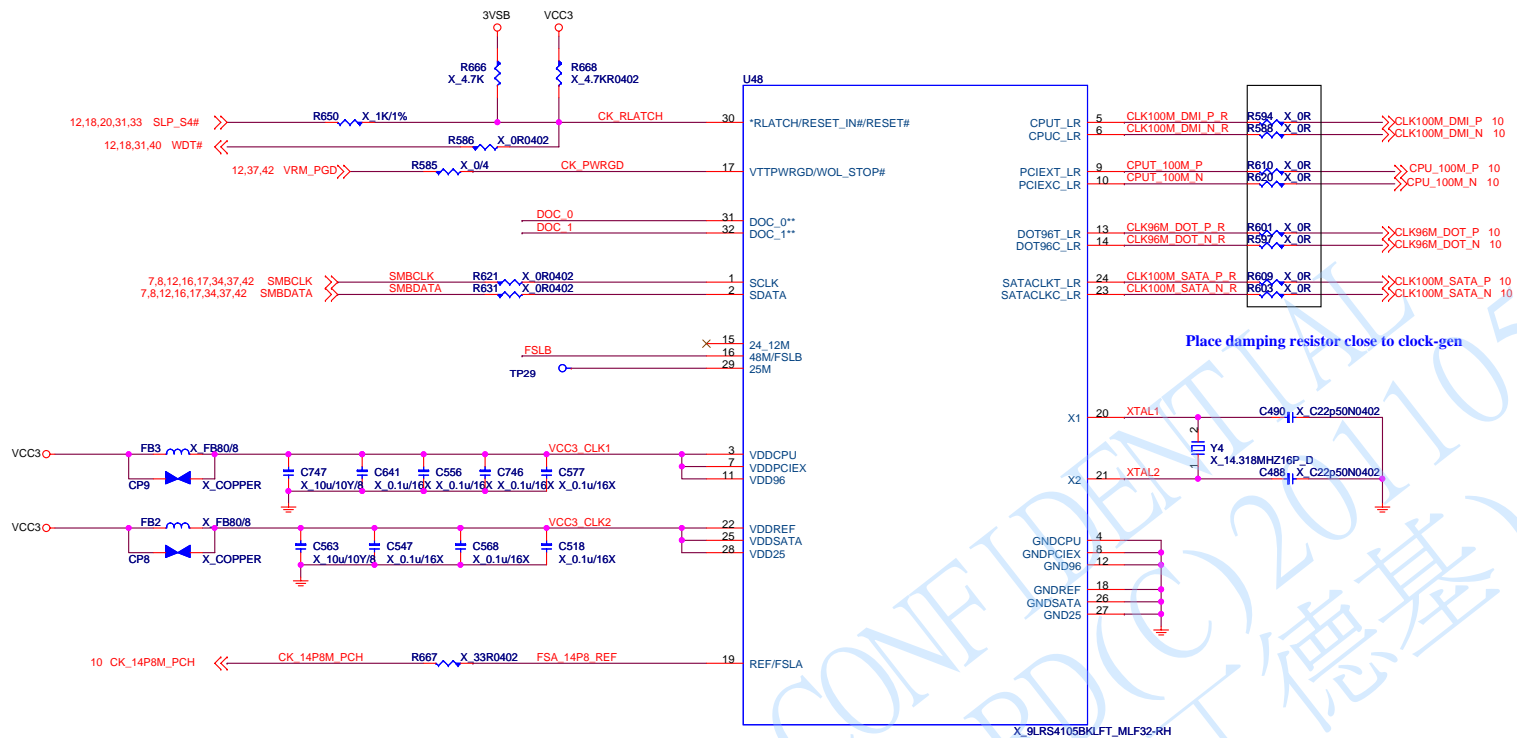


# DDRIII DIMM\_B0

# DDRIII DIMM\_B1

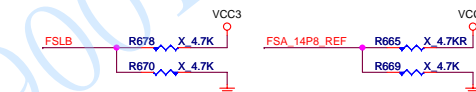






# CLOCK GEN STRAPPING

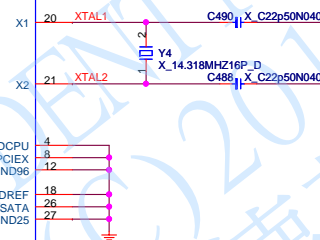
FS4	FS3	FS2	FSB	FSA	CPU	Spread
B0b4	B0b3	B0b2	B0b1	B0b0	Mhz	%
0	0	0	0	0	100.00	-0.5
0	0	0	0	1	133.33	-0.5
0	0	0	1	0	200.00	-0.5
0	0	0	1	1	166.66	-0.5



Pin16: 48MHz clock output. / 3.3V tolerant input for CPU frequency selection. Low voltage threshold inputs, see input electrical characteristics for Vil\_FS and Vih\_FS values.

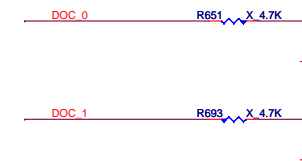
Pin19: 14.318 Mhz reference clock. / 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil\_FS and Vih\_FS values.

Place damping resistor close to clock-gen

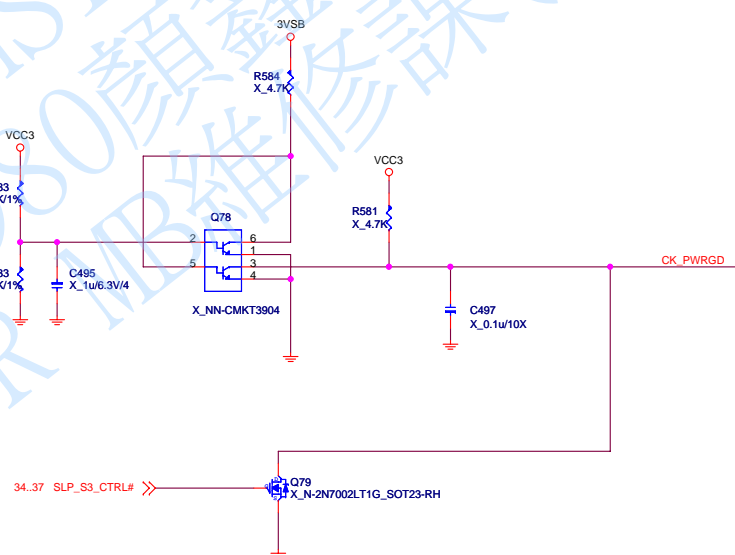
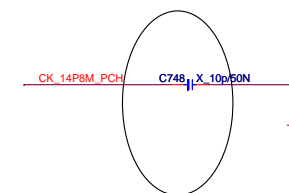


## OC

DOC\_0\*\*:Dynamic Over Clocking pin: real time frequency selection 0: Normal; 1: Frequency will transition to a preprogrammed value in the I2C.



## EMI

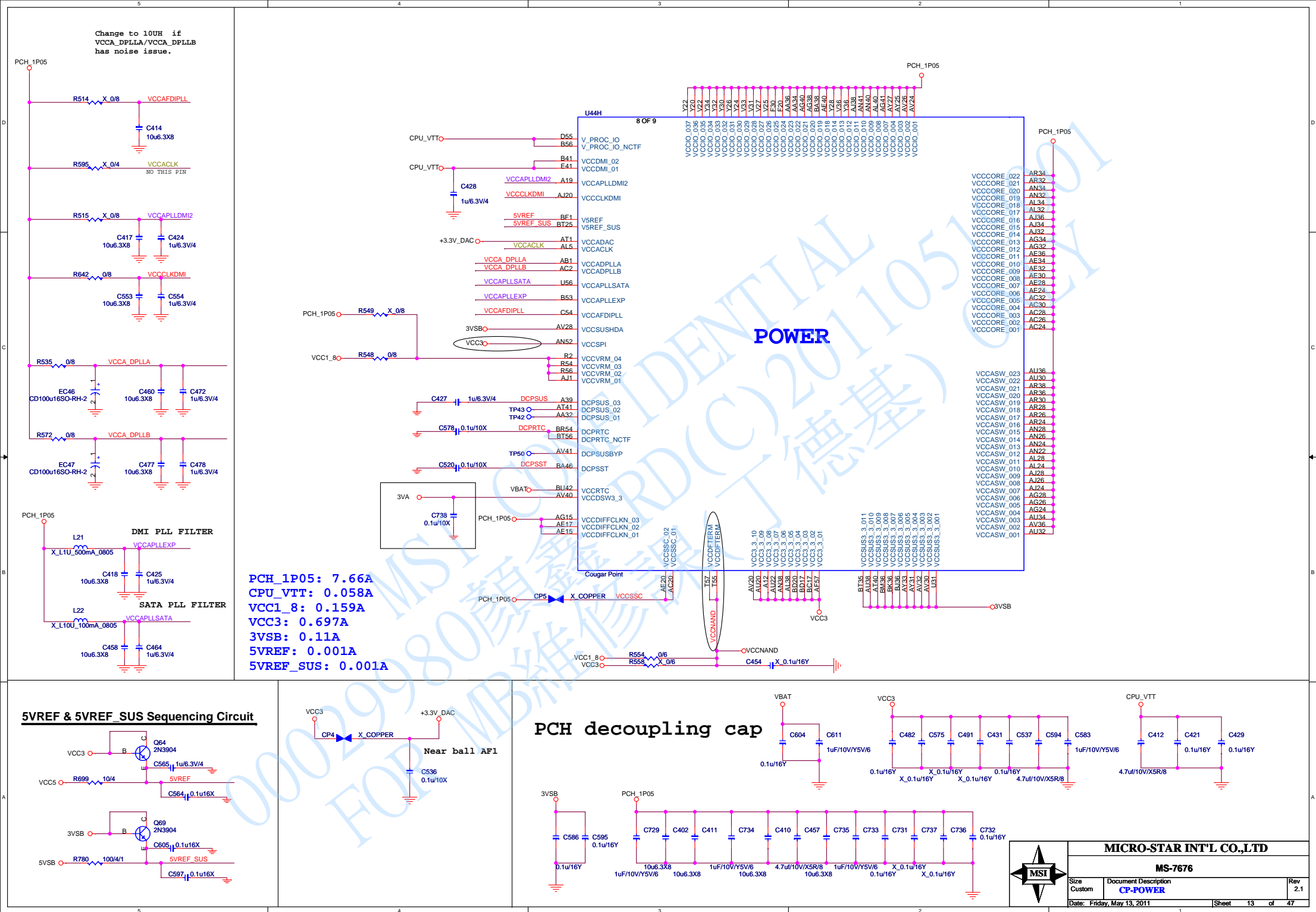


MICRO-STAR INT'L CO.,LTD			
MS-7676			
Size	Document Description	Rev	
Custom	CLK GEN4105	2.1	
Date:	Friday, May 13, 2011	Sheet	9 of 47

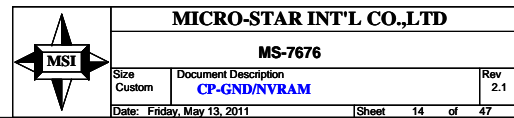






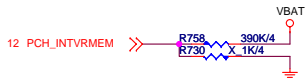
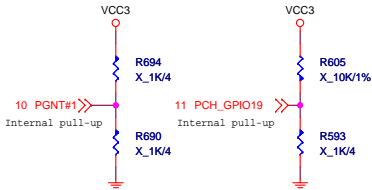






PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



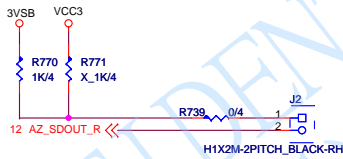
INTVRMEN  
0: DISABLE INTERNAL VRM  
1: ENABLE INTERNAL VRM \*

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



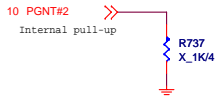
DSWVRMEN  
0 : Disable Internal Deep Sleep 1.05 V regulators.  
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.

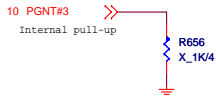


HDA\_SDO  
Disable ME in Manufacturing Mode when pull LOW ????

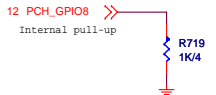
HDA\_SDO has internal pull down.  
Default should be connected to SDIN of codec, no pull up/down.  
To Disable ME need to have a jumper to pull high



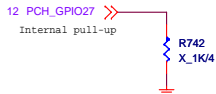
DMI AC/DC MODE  
0 : AC  
1 : DC \*



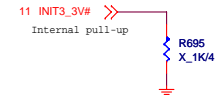
Topblock swap override when pull-low  
Signal has a weak internal pull-up



GPIO8  
0 : Integrated Clocking Enable (FCIM) \*  
1 : Buffer Through Mode Enable (BTM)

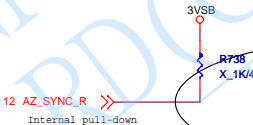


GPIO28  
0 : OD PLL VR disabled  
1 : OD PLL VR enabled \*  
Signal has a weak internal pull-up



INIT3\_3V#  
0 : ??????????????  
1 : ?????????????? \*

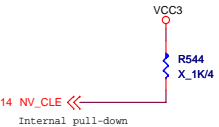
1: INIT3\_3V to asserted for 16 PCI clock to reset the processor by some evens occur.  
0: Can not to reset the processor.



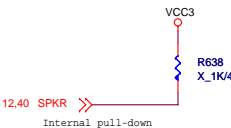
HDA\_SYNC  
OD PLL VR SUPPLY SEL  
0: 1.8V SUPPLY \*  
1: 1.5V SUPPLY



GPIO15  
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY \*  
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE  
DC COUPLED: TX/RX TO VCC IF SAMPLED HIGH  
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW \*?  
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

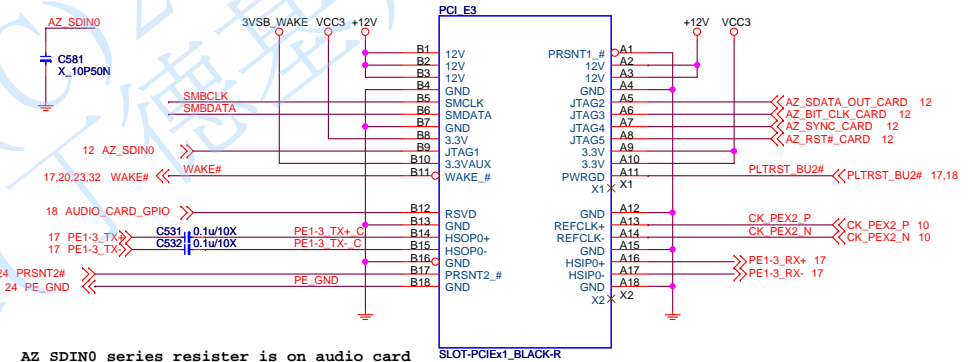
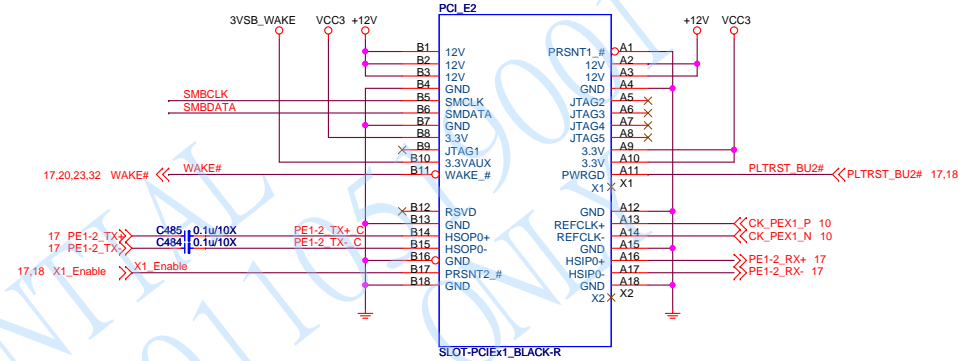
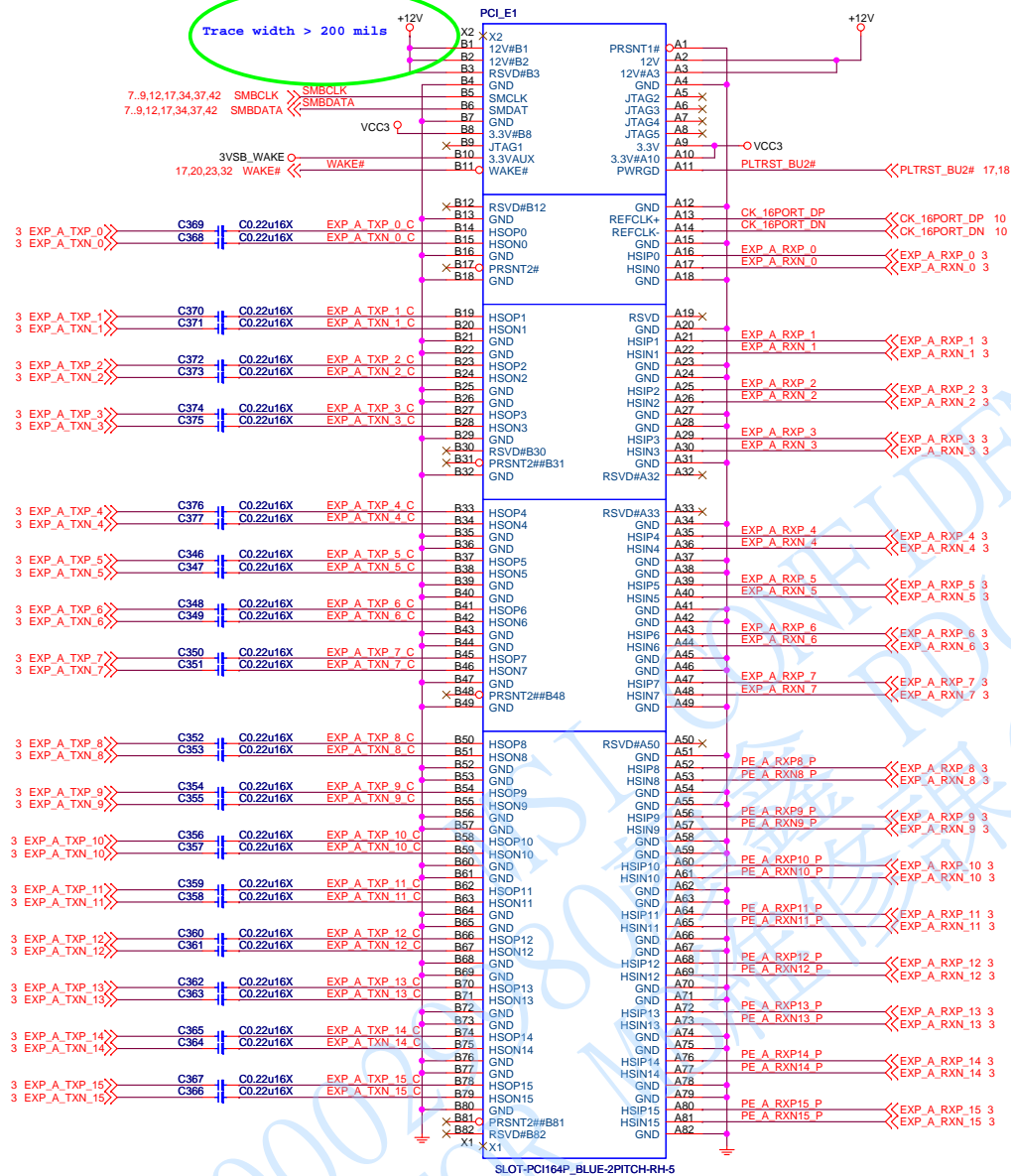


SPKR  
0 : EN TCO REBOOT \*  
1 : DIS TCO REBOOT



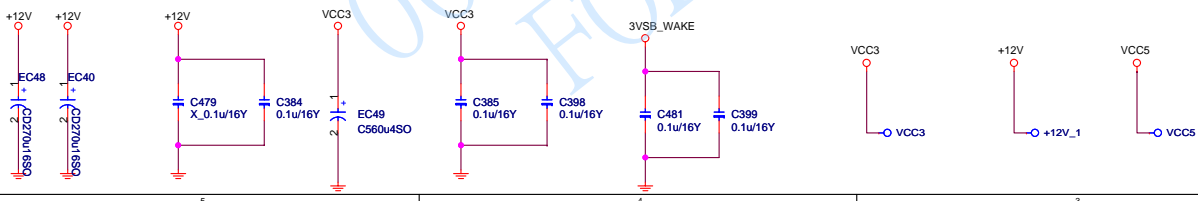
MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size Custom	Document Description CP-Strap	Rev 2.1
Date: Friday, May 13, 2011		Sheet 15 of 47

PCI\_Express X16 Slot



AZ\_SDIN0 series resister is on audio card

```
AUDIO_CARD_GPIO
HI:LED OFF
LOW:LED ON
```

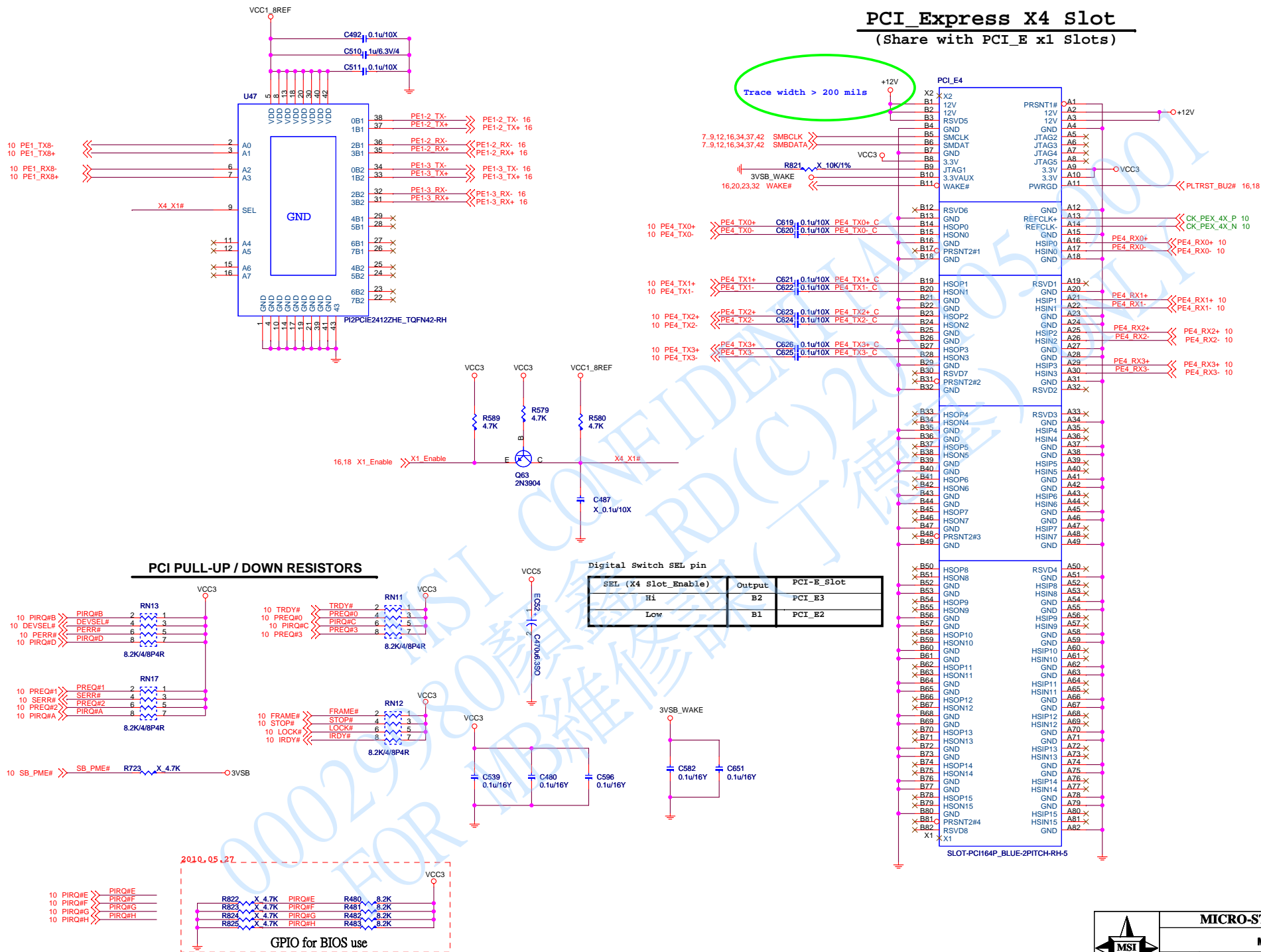


**MICRO-STAR INT'L CO.,LTD**

MS-7676

Size Custom	Document Description <b>PCIE x16 /x1 /x1HDA CO-LAY</b>	Rev 2.1
Date: Friday, May 13, 2011	Sheet 16 of 47	

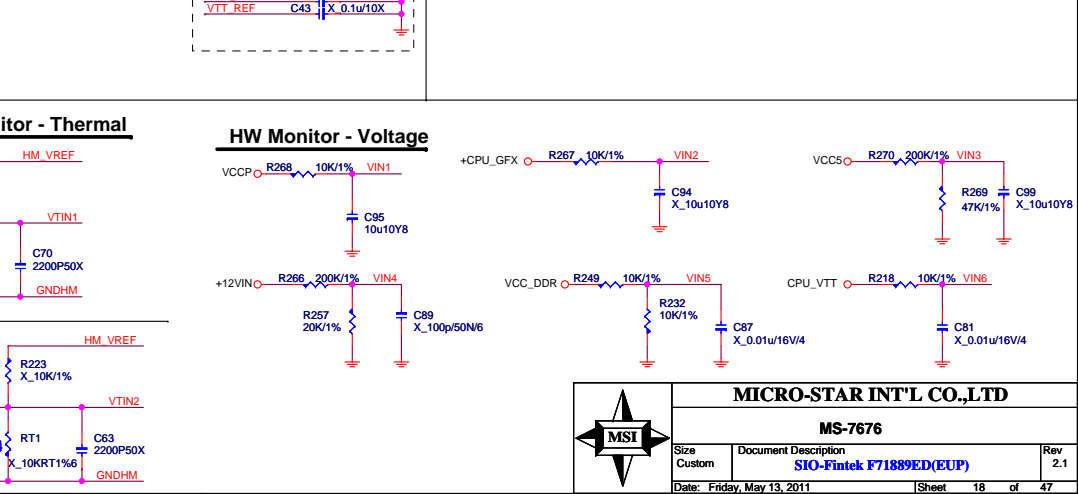
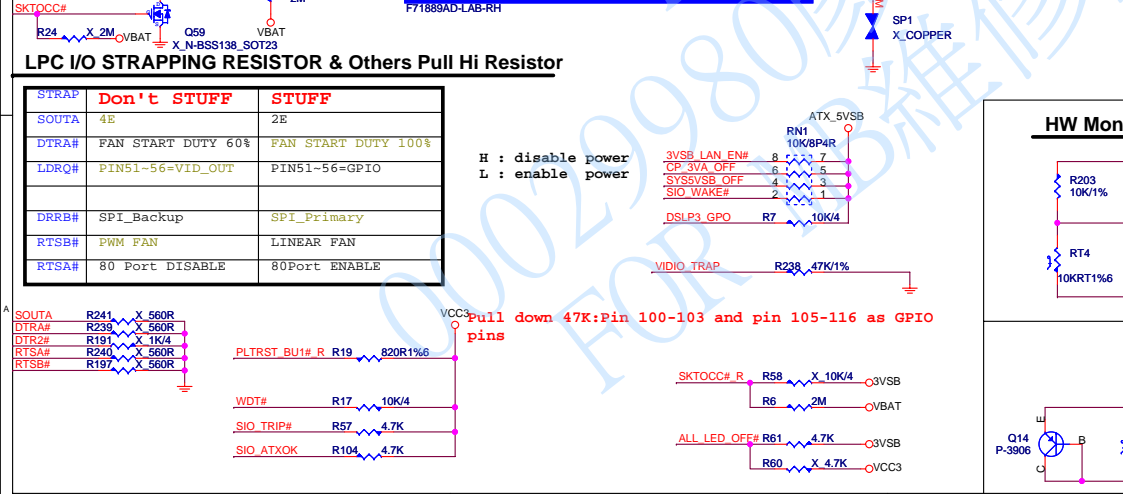
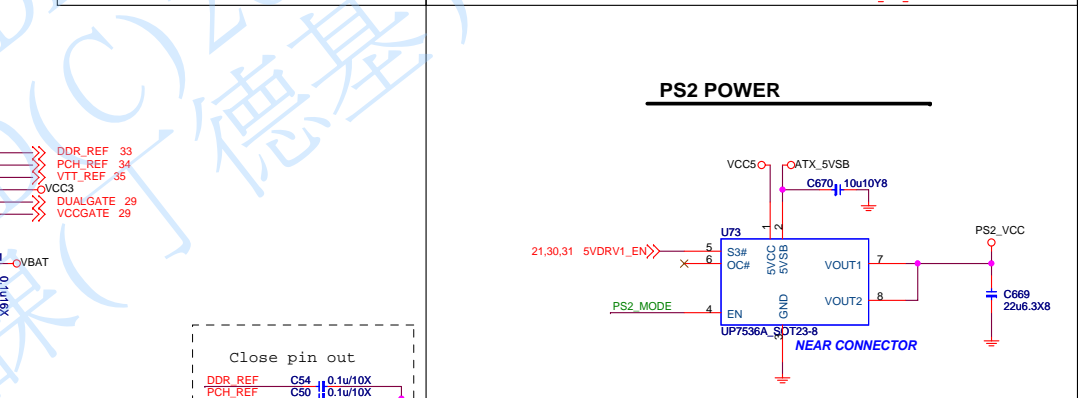
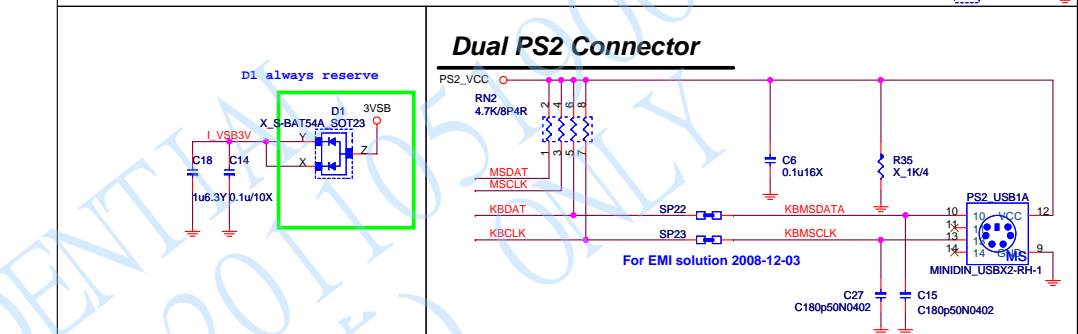
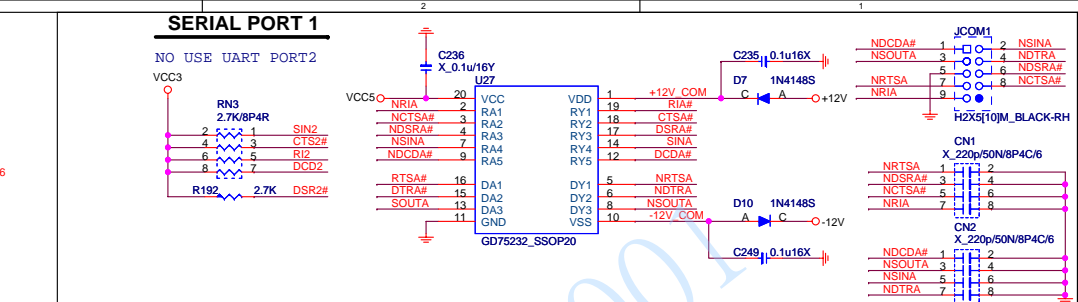
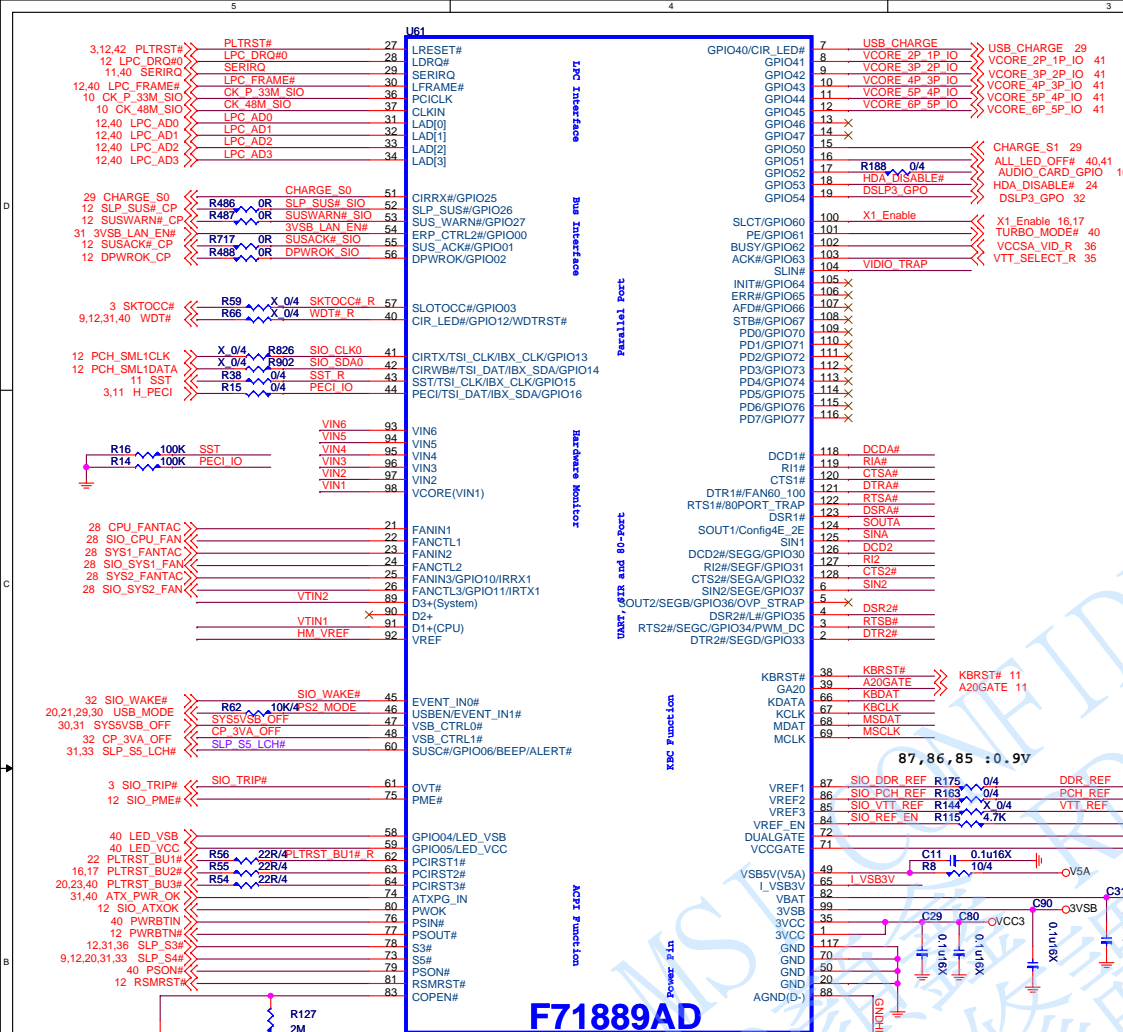
# PCI Express X4 Slot (Share with PCI\_E x1 Slots)



MICRO-STAR INT'L CO.,LTD


MS-7676

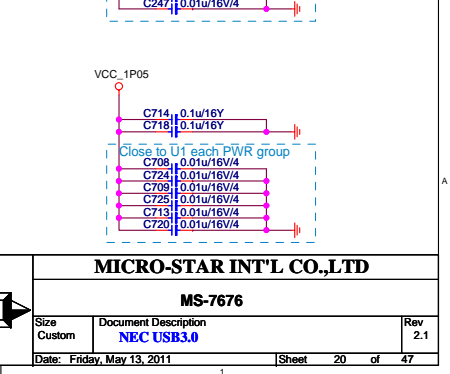
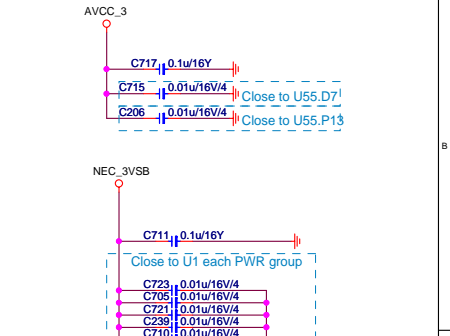
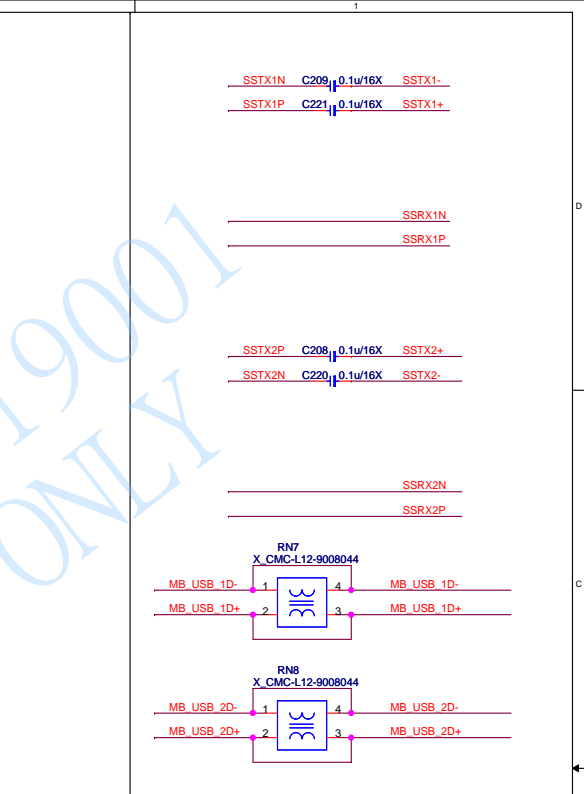
Size	Document Description	Rev
Custom	PCIe4 Slots	2.1
Date: Friday, May 13, 2011	Sheet 17 of 47	

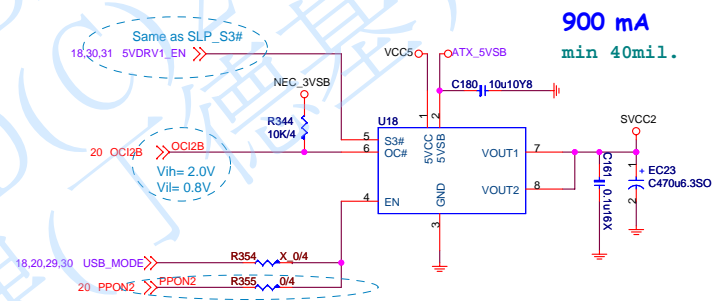




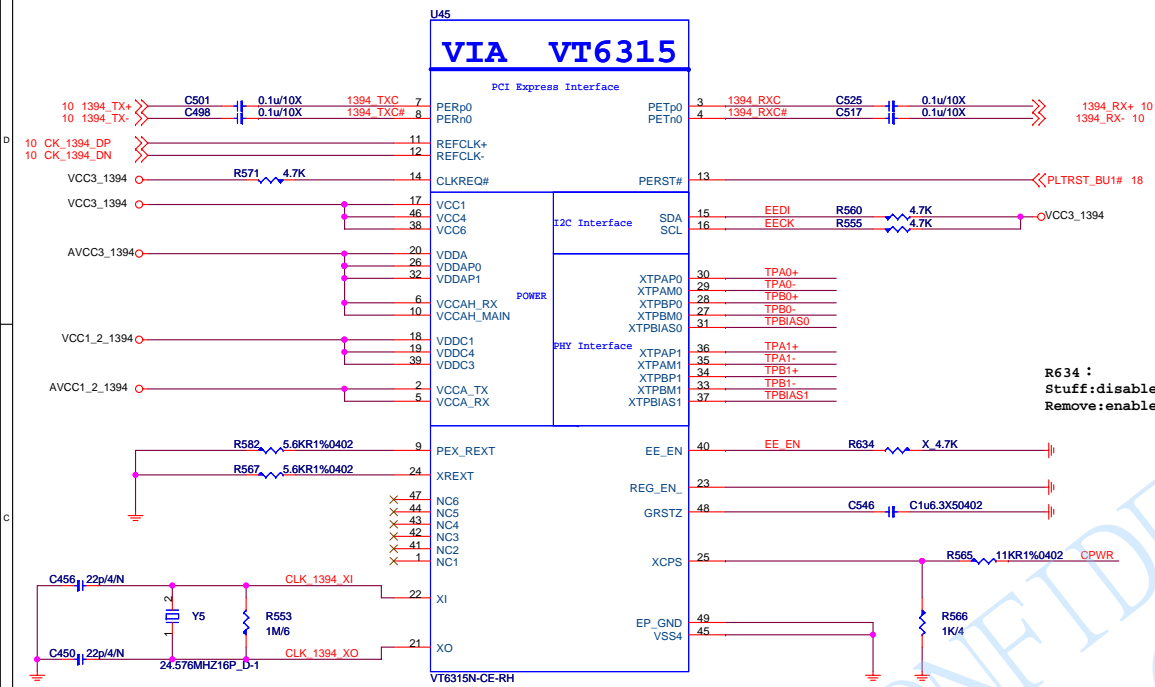
MSI CONFIDENTIAL  
00029980 顏鑫 RD(C)20110519001  
FOR MB維修課(丁德基) ONLY

			MICRO-STAR INT'L CO.,LTD	
			MS-7676	
Size	Document Description			Rev
Custom	MARVELL SATA 6G			2.1
Date: Friday, May 13, 2011		Sheet	19	of 47

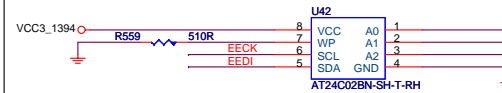




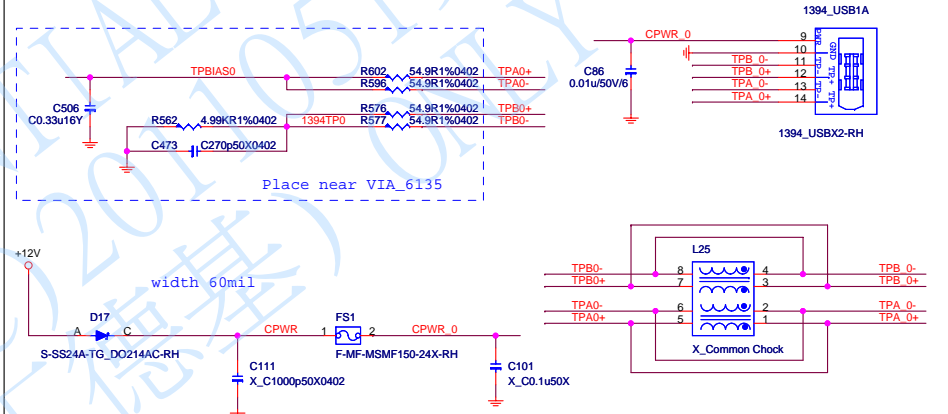
# 1394 CONTROLLER



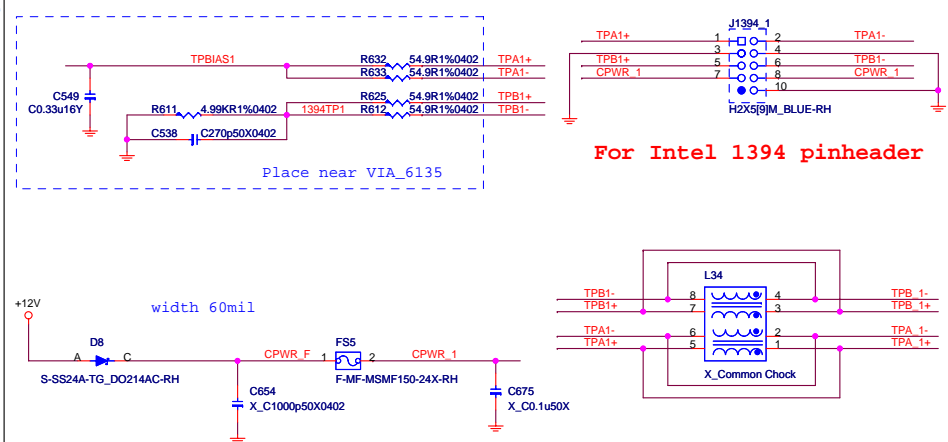
## EE PROM



## Rear 1394 port

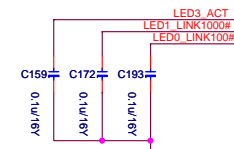
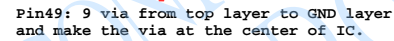


## Front 1394 pin header



MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size	Document Description	Rev
Custom	1394 Controller - VT6315N-CE	2.1
Date: Friday, May 13, 2011	Sheet 22 of 47	

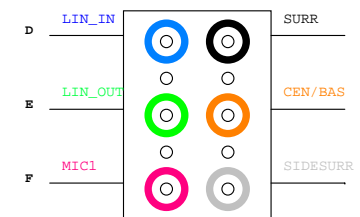
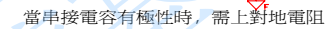
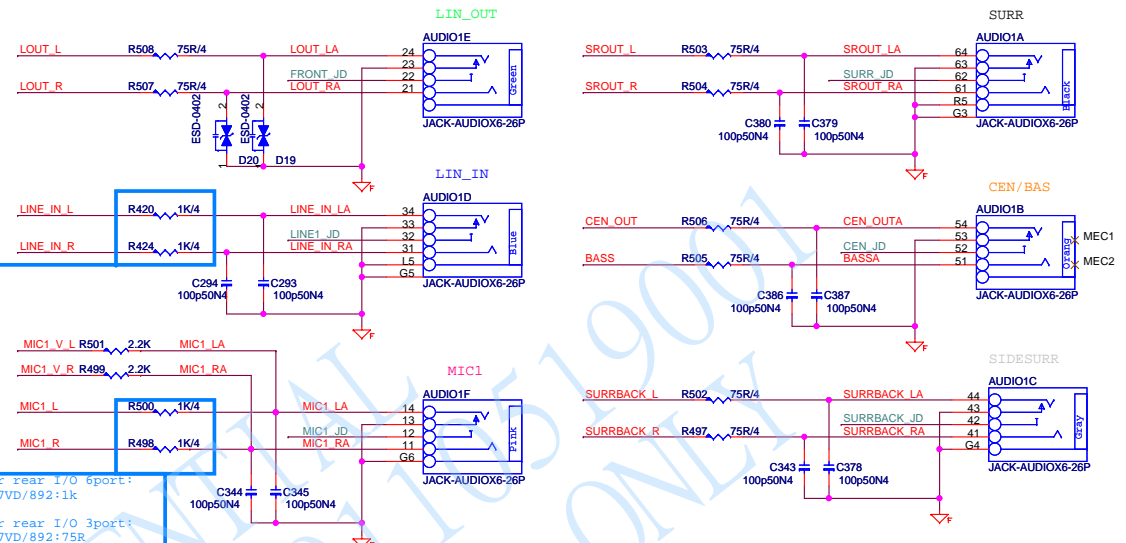
RTL8105E 10/100M LAN



Size Custom	Document Description <b>LAN - RTL8111E</b>	Rev 2.1
Date: Friday, May 13, 2011		Sheet 23 of 47



## ALC892



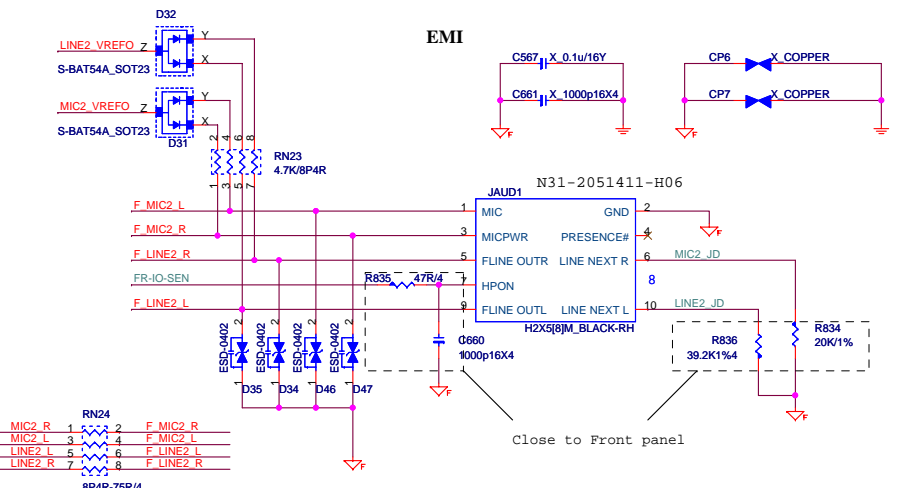
**SENSE A**

R727	5.1K1%4	FRONT_JD
R751	10K1%1	LINE1_JD
R720	20K1%1	MIC1_JD
R750	39.2K1%4	SURR_JD

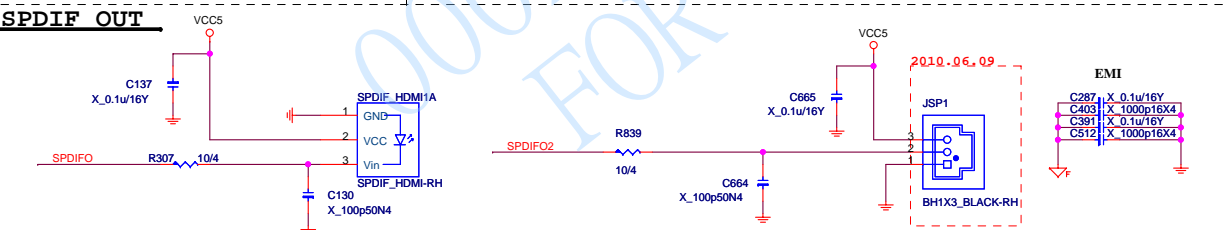
**Closed Codec**

**SENSE B**

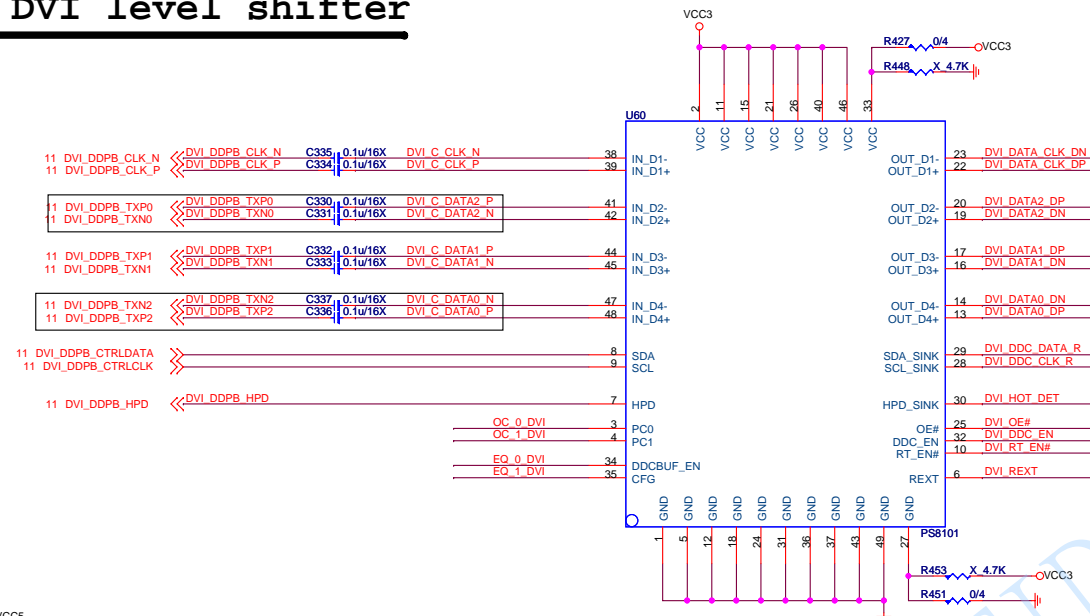
R804	10K1%1	CEN_JD
R805	5.1K1%4	SURRBACK_JD
R811	X Short	FR-IO-SEN



SPDIF OUT



# DVI level shifter

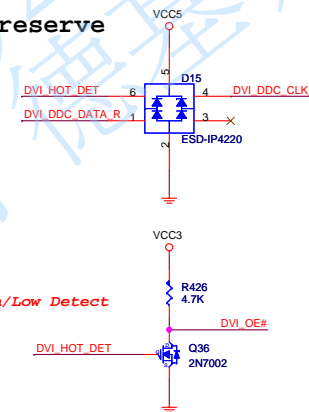


PERICOM料號: B0B-411LS2C-P22.  
PARADE料號: B0B-081010C-P97.

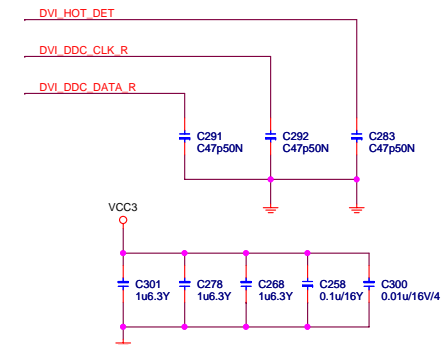
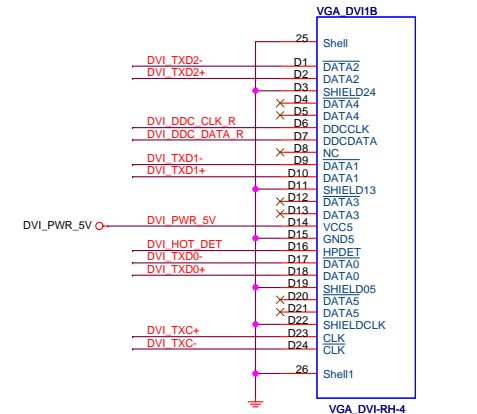
Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMDSB_DATA2#	DDPB_ON
	DDSP_B_TX0_DP	TMDSB_DATA2	DDPB_OP
	DDSP_B_TX1_DN	TMDSB_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMDSB_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMDSB_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMDSB_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMDSB_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMDSB_CLK	DDPB_3P
	DDPB_HPDP	DDSP_B_HPDP0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMI_CTRL_DATA	

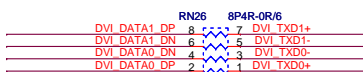
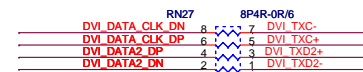
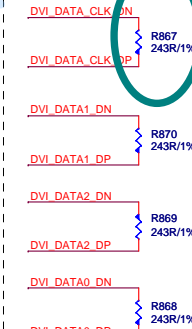
reserve



注意High/Low Detect



EMI



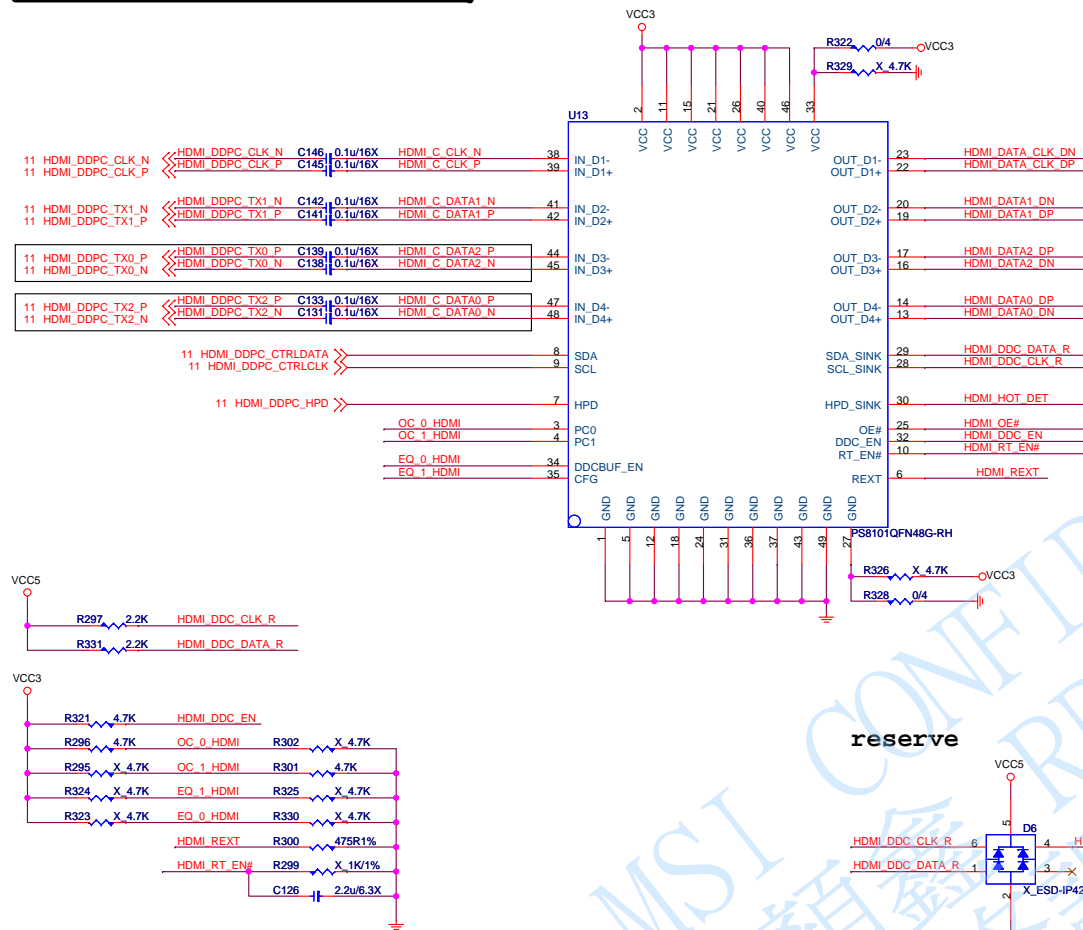
	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0	note
00	8 dB
01	4 dB
10	12 dB
11	0 dB

**MICRO-STAR INT'L CO.,LTD**  
**MS-7676**  
Size Custom | Document Description **DVI transfer** | Rev 2.1  
Date: Friday, May 13, 2011 | Sheet 25 of 47

# HDMI level shifter



reserve

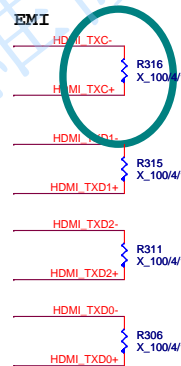
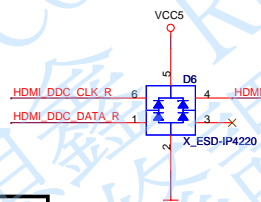
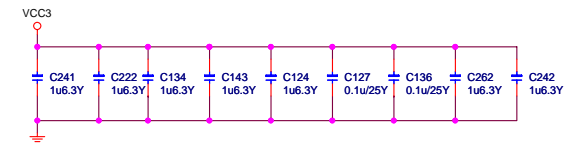
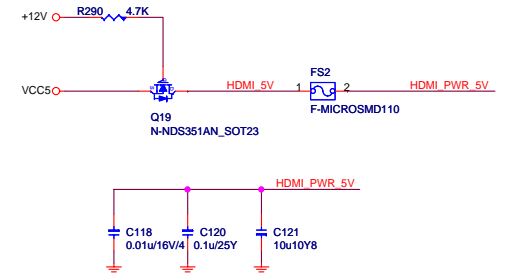
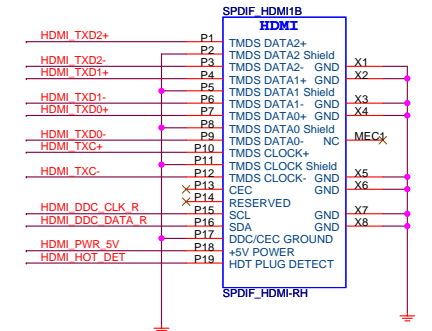
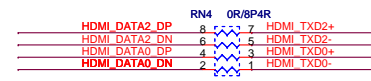
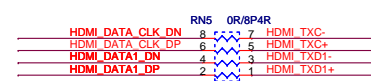
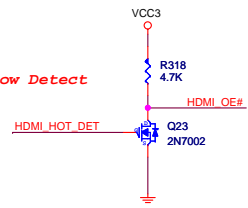


Table 8-1. PCH PCI Express Tx/RX - HDMI Signal Mappings

Port	Digital Display Interface Differential Pairs	HDMI Signals	PCH Digital Display Interface Pins
Port B	DDSP_B_TX0_DN	TMD0B_DATA2#	DDPB_ON
	DDSP_B_TX0_DP	TMD0B_DATA2	DDPB_OP
	DDSP_B_TX1_DN	TMD0B_DATA1#	DDPB_1N
	DDSP_B_TX1_DP	TMD0B_DATA1	DDPB_1P
	DDSP_B_TX2_DN	TMD0B_DATA0#	DDPB_2N
	DDSP_B_TX2_DP	TMD0B_DATA0	DDPB_2P
	DDSP_B_TX3_DN	TMD0B_CLK#	DDPB_3N
	DDSP_B_TX3_DP	TMD0B_CLK	DDPB_3P
	DDPB_HPD	DDSP_B_HPD0	Hot plug detect used by HDMI Port B.
	SDVO_CTRLCLK	HDMI0_CTRL_CLK	HDMI DDC lines for Port B
	SDVO_CTRLDATA	HDMI0_CTRL_DATA	



注意High/Low Detect



	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

**MICRO-STAR INT'L CO.,LTD**

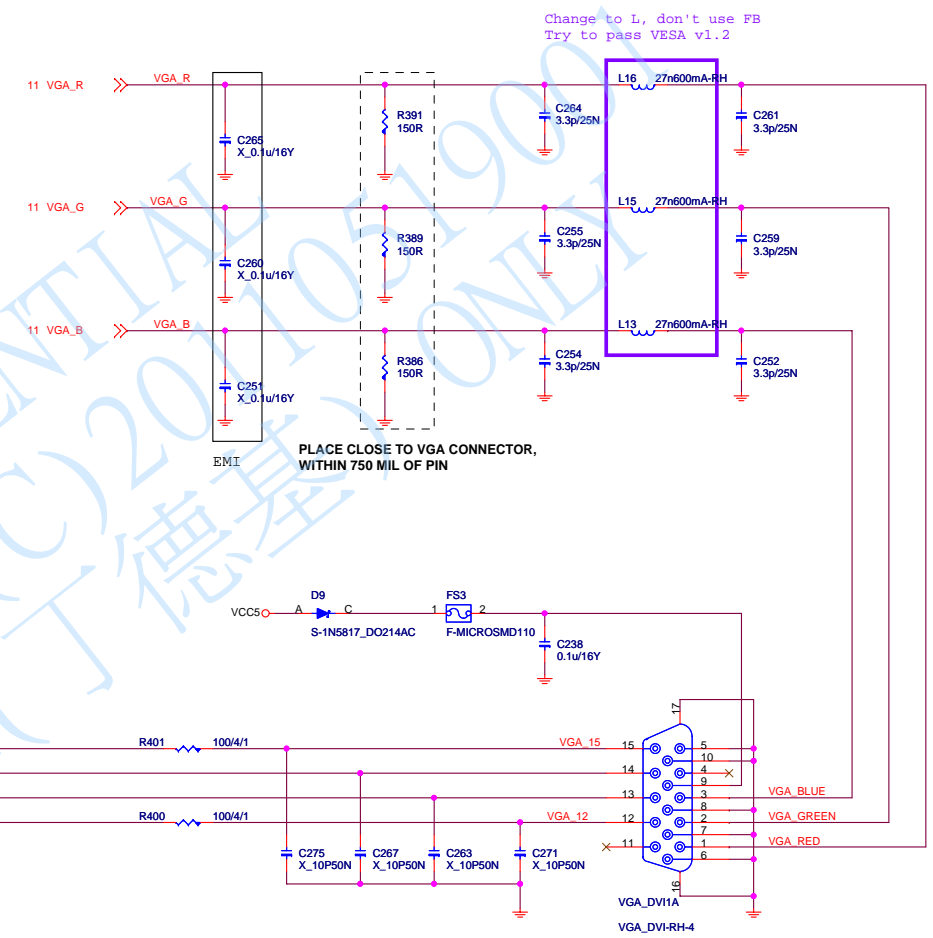
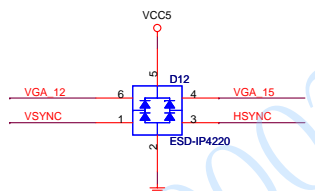
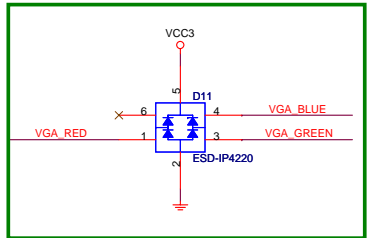
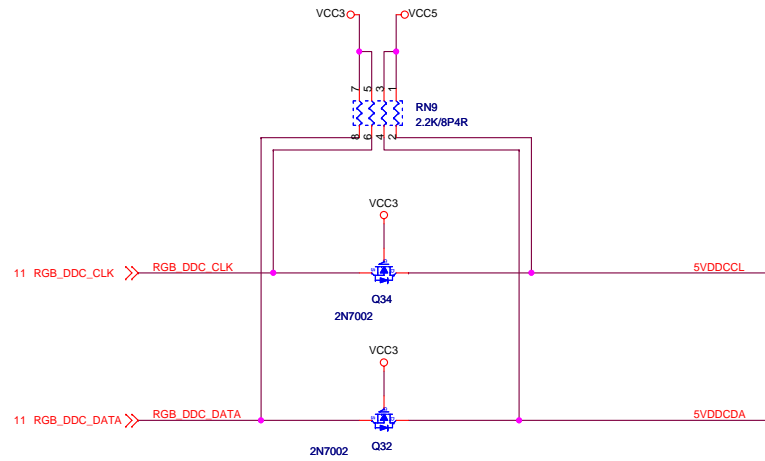
**MS-7676**


Size Custom Document Description **HDMI** Rev 2.1

Date: Friday, May 13, 2011 Sheet 26 of 47

D-Sub

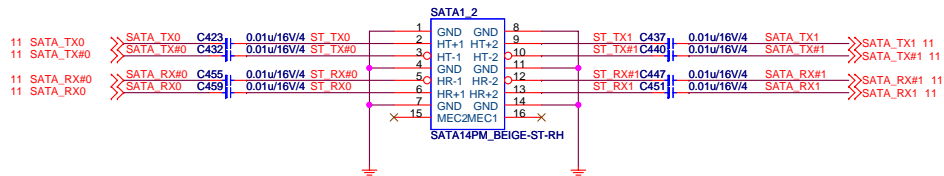
Level shift



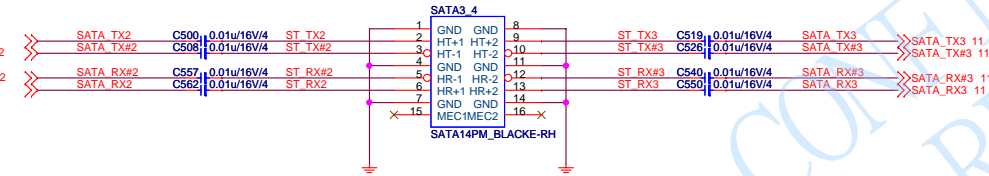


MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size	Document Description	Rev
Custom	VGA	2.1
Date: Friday, May 13, 2011		Sheet 27 of 47

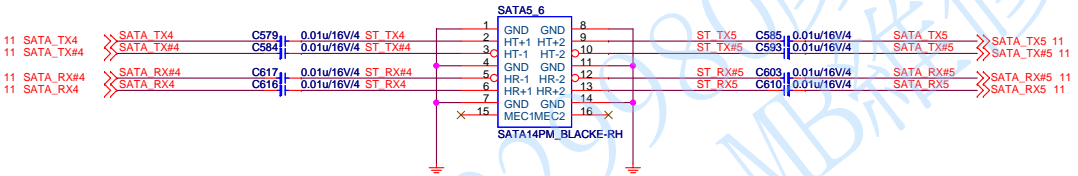
### SATA 6G PORT 0,1



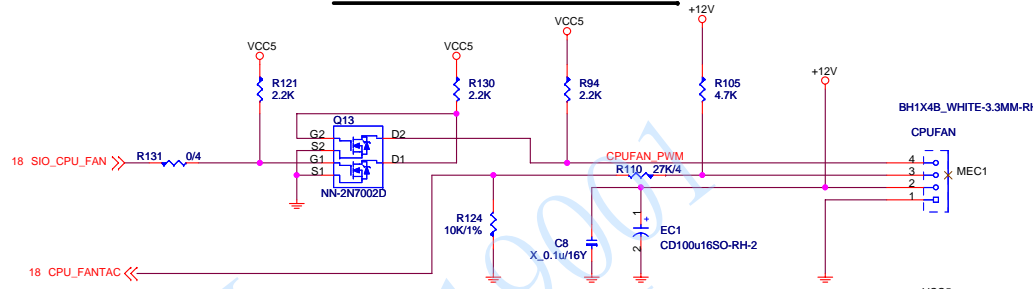
### SATA 3G PORT 2,3



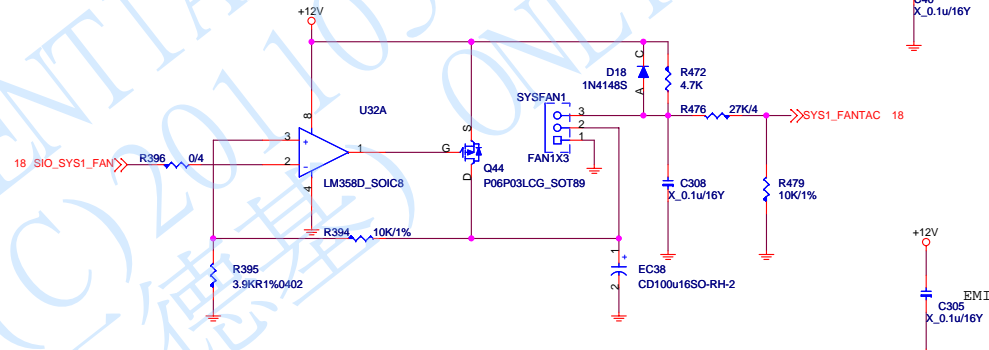
### SATA 3G PORT 4,5



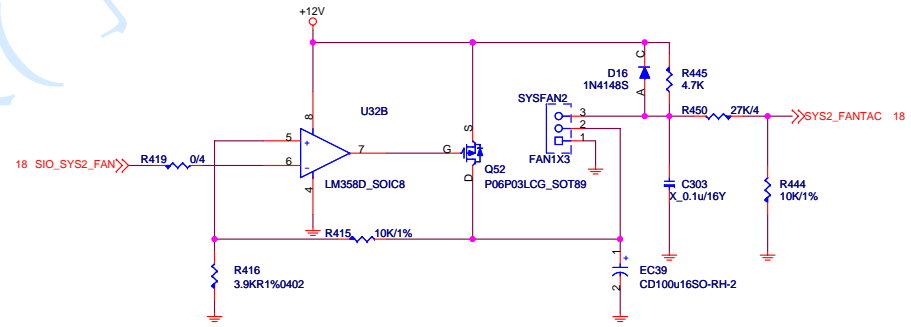
### CPU FAN-COUNTROL CIRCUIT



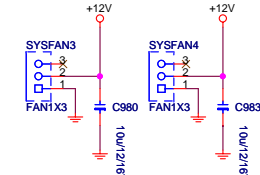
### SYSTEM FAN1-COUNTROL CIRCUIT



### SYSTEM FAN2-COUNTROL CIRCUIT



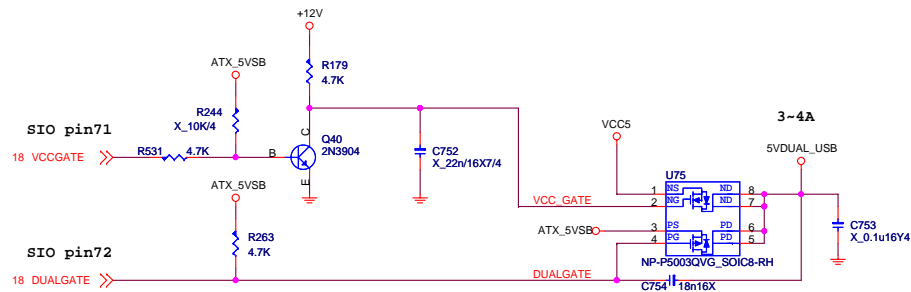
### SYSTEM FAN3-12V



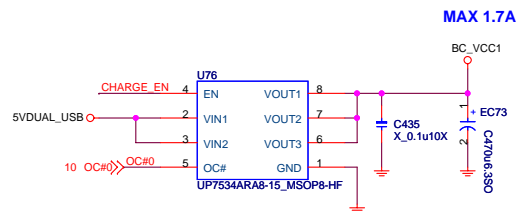
MICRO-STAR INT'L CO.,LTD			
MS-7676			
Size	Document Description	Rev	
Custom	SATA / FAN Control	2.1	
Date:	Friday, May 13, 2011	Sheet	28 of 47



## 5VDUAL\_USB



## USB POWER FOR PORT 0 for USBCharging



SIO GPIO40 Pin7 (I\_VSB3V)

USB\_CHARGE: (OD)

0: Don't support USB charge and resume.

1: Support USB charge and resume.

Power plug in , H/W default support USB charge.

SIO GPIO25 (I\_VSB3V)

SIO GPIO50 (I\_VSB3V)

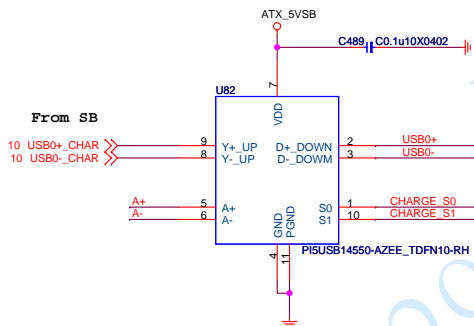
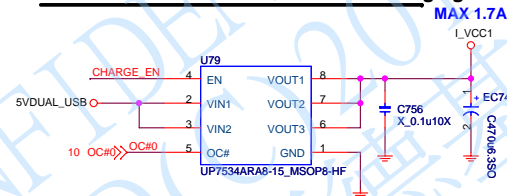
CHARGE\_S1: (PUSH PULL)

CHARGE\_S0: (OPEN DRAIN ONLY)

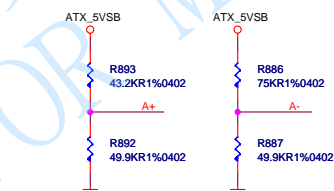
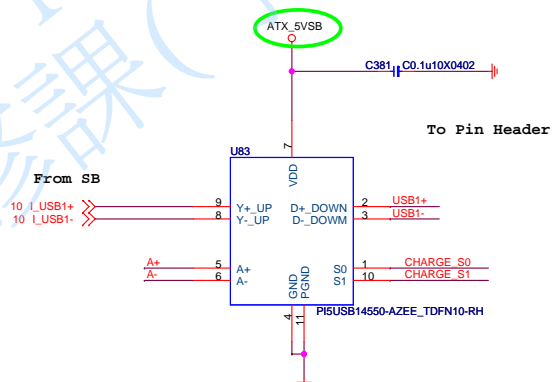
	S0	S1
AUTO:	0	0
DCP :	0	1
A :	1	0
Y :	1	1

H/W default support auto charging in S3/S4/S5 and usb link in S0.

## USB POWER FOR PORT 1 for USBCharging



S1	0	0	1
S0	0	1	1
Mod	AUTO	A	V

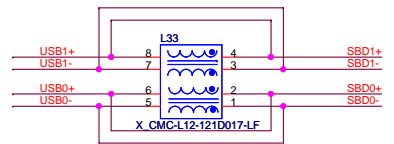
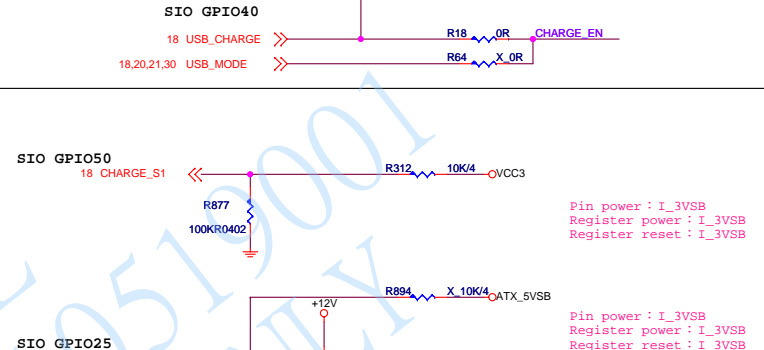


A type

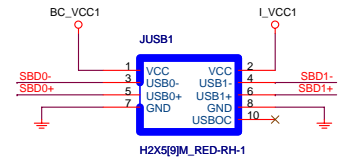
2.70V< D+ <3.1 V \*

1.85V< D- < 2.1V \*

For i-Pad / i-Phone 4G charges current up to 1.6A.



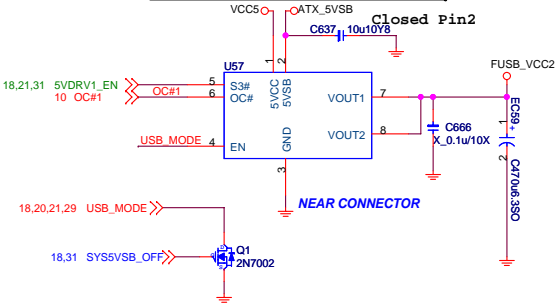
PI5USB14550 has internal EDS diode.



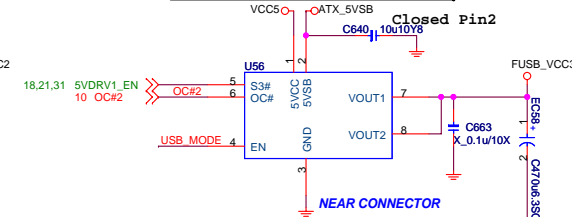
MICRO-STAR INT'L CO.,LTD			
MS-7676			
Size	Document Description	Rev	
Custom	USB Charger	2.1	
Date:	Friday, May 13, 2011	Sheet	29 of 47

# Front USB Connector

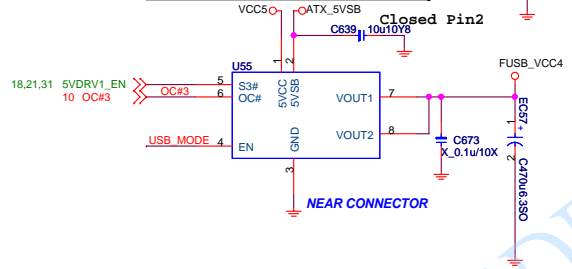
## USB POWER REAL PORT 2,3



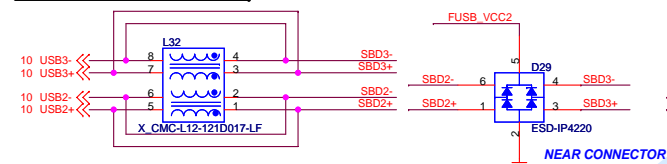
## USB POWER FOR PORT 4,5



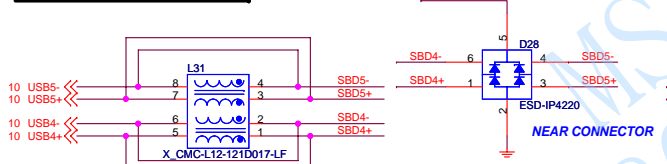
## USB POWER FOR PORT 6,7



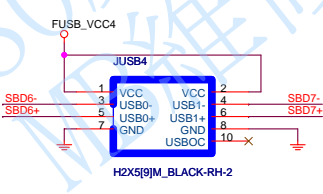
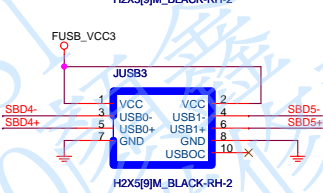
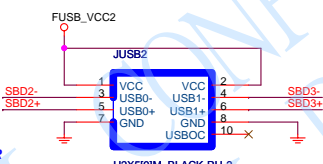
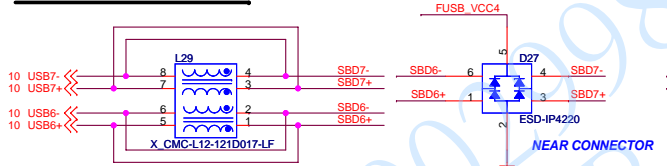
## FRONT USB PORT 2,3



## FRONT USB PORT 4,5

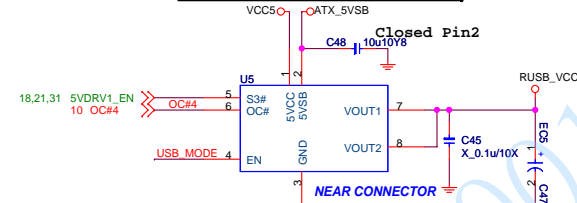


## FRONT USB PORT 6,7

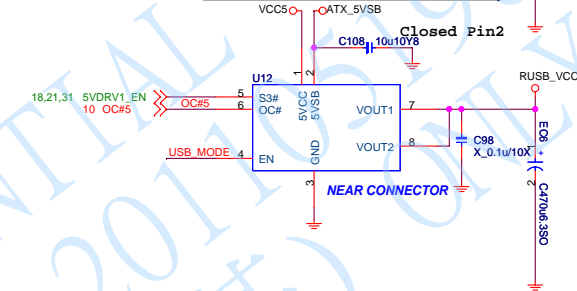


# Rear USB Connector

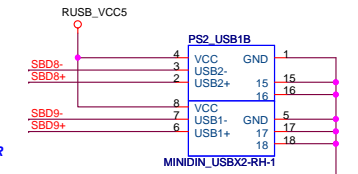
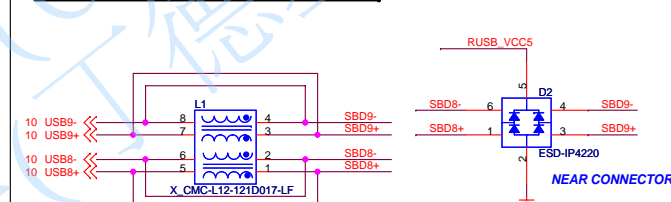
## USB POWER FOR PORT 6,7



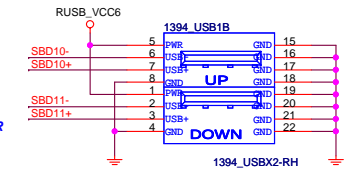
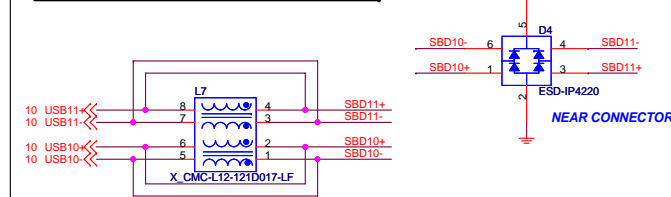
## USB POWER FOR PORT 8,9



## REAR USB PORT 8,9 (With PS2)



## REAR USB PORT 10,11 (With 1394)



USB\_MODE for USB voltage  
H:Follow 5VSB  
L:Always off

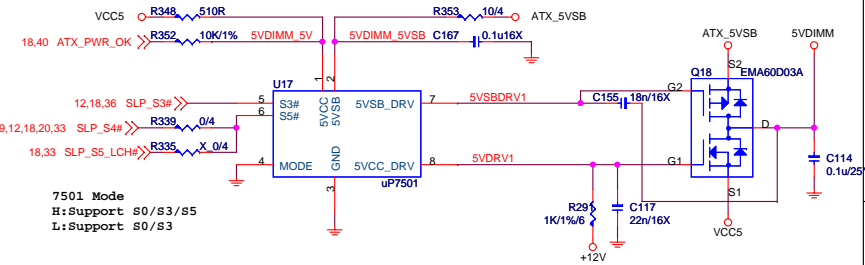


MICRO-STAR INT'L CO.,LTD

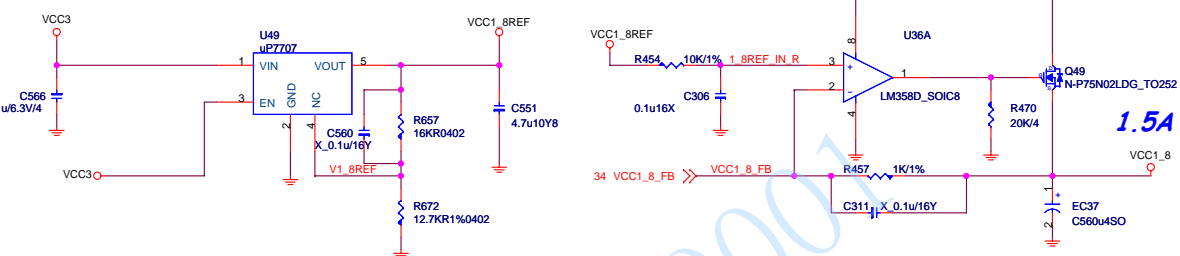
MS-7676

Size	Document Description	Rev
Custom	USB Connector	2.1
Date: Friday, May 13, 2011	Sheet 30 of 47	

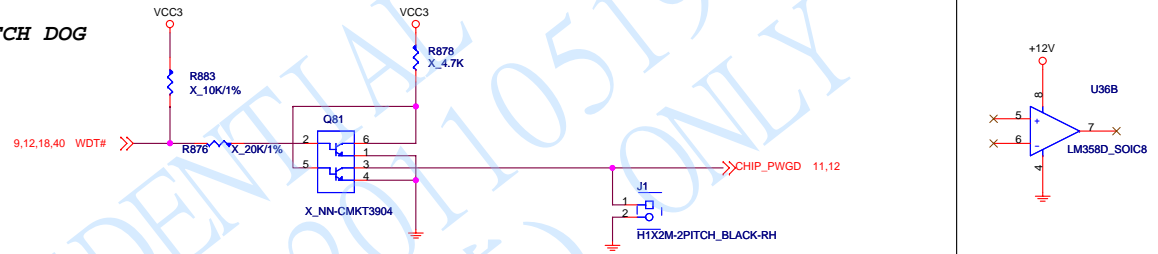
5VDIMM FOR DDR



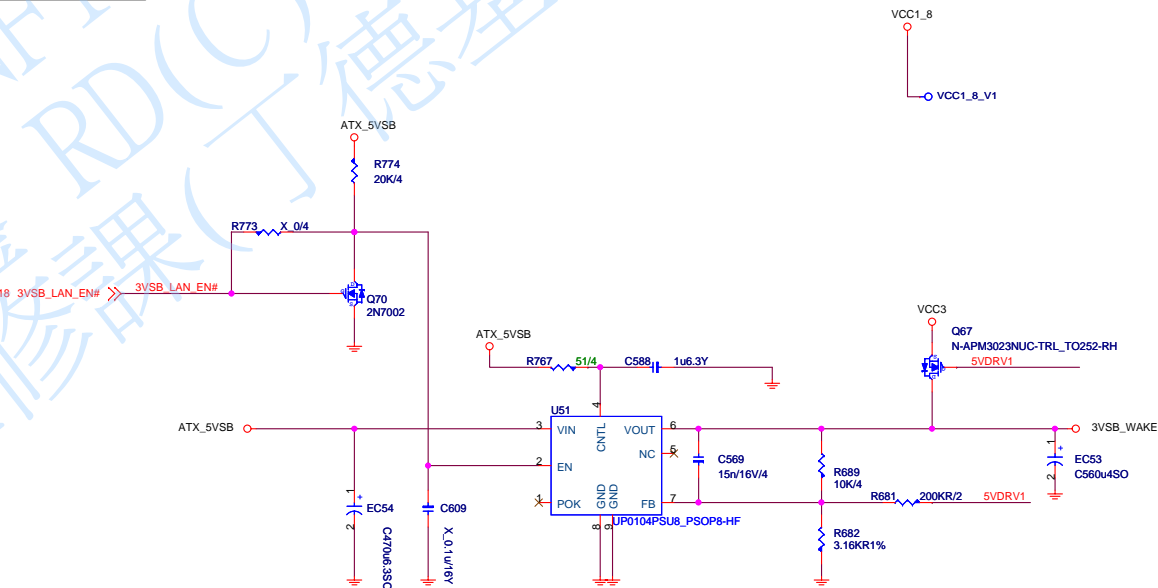
VCC1\_8REF



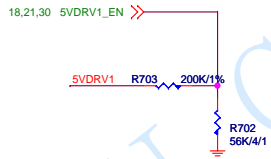
WATCH DOG



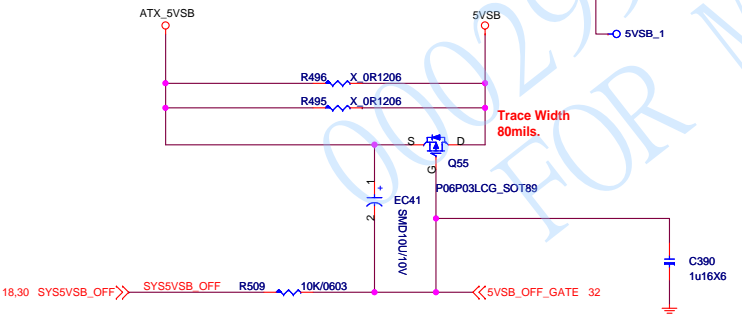
3VSB\_WAKE




USB MODE



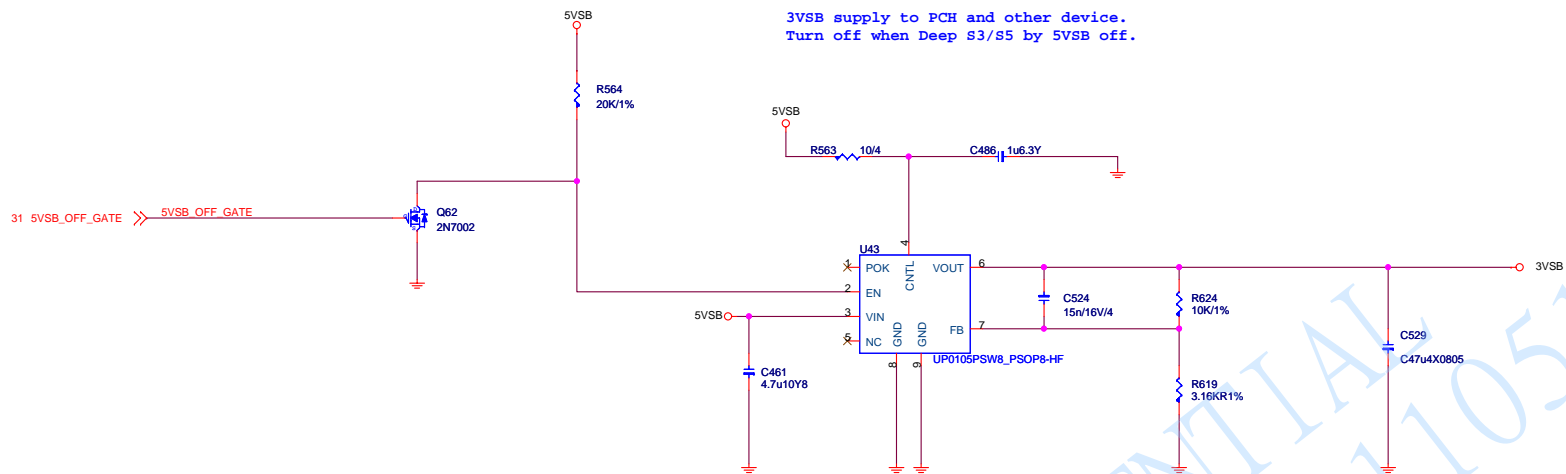
5VSB Power Switch



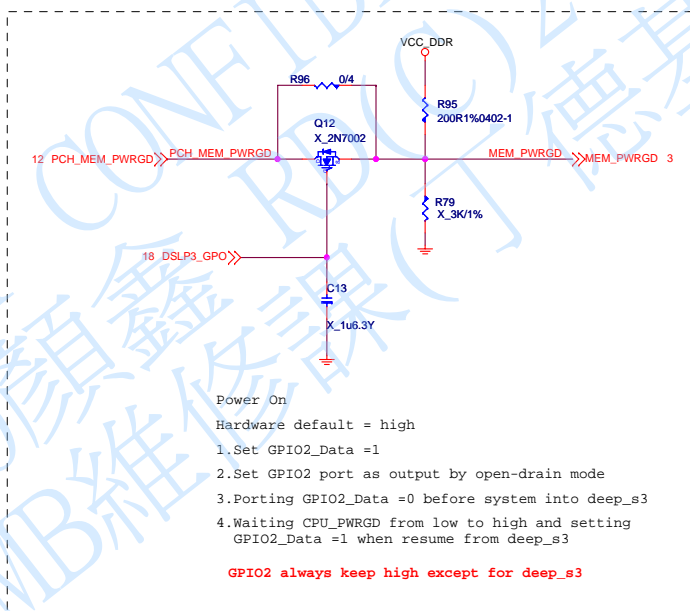
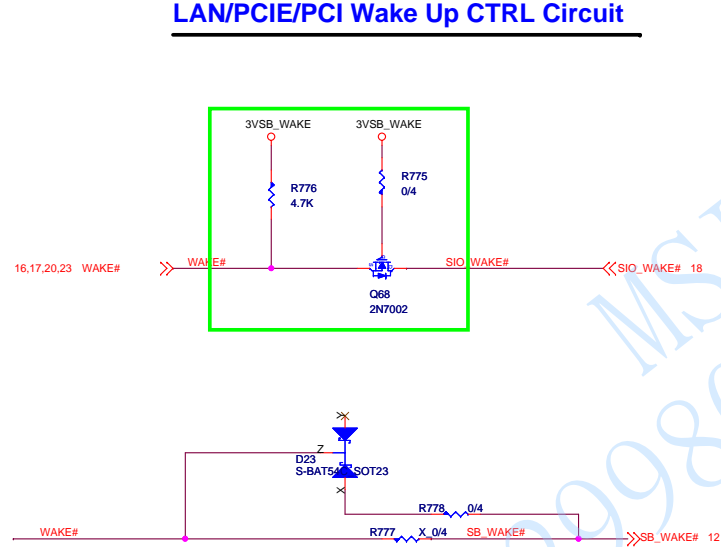


MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size	Document Description	Rev
Custom	ACPI controller UPI	2.1
Date: Friday, May 13, 2011	Sheet 31 of 47	

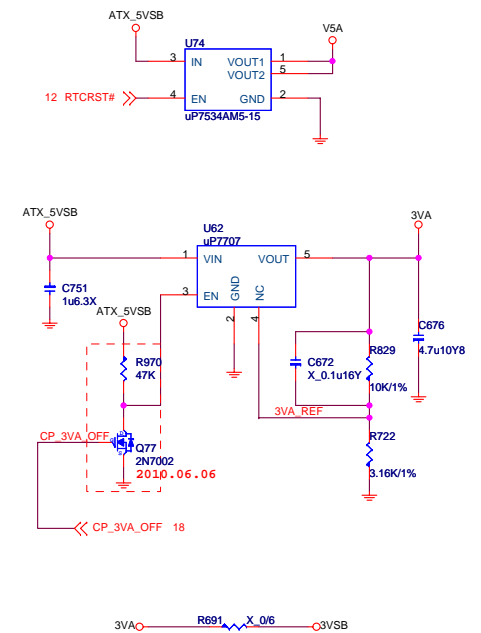
## Deep Mode WOL LAN Power CTRL Circuit



## LAN/PCIE/PCI Wake Up CTRL Circuit



## RTRCRST patch circuit for clr-CMOS PCH will wake up issue



DDR Power:1.5V

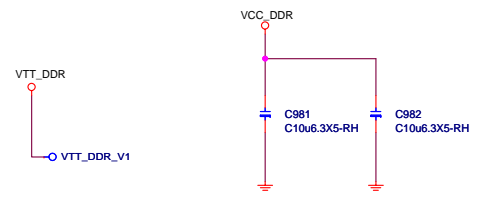
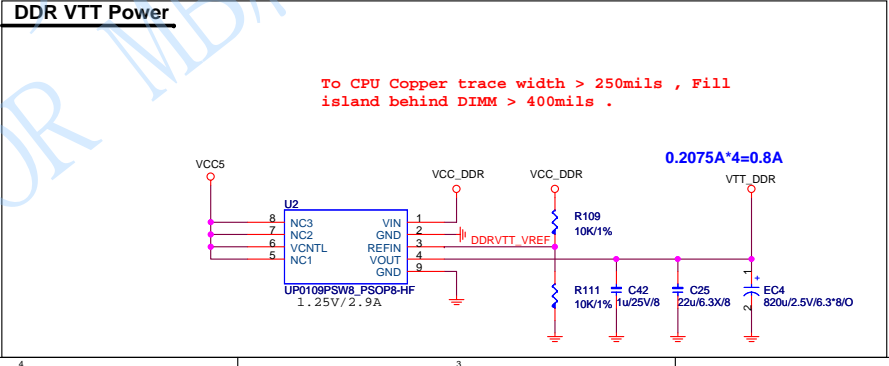
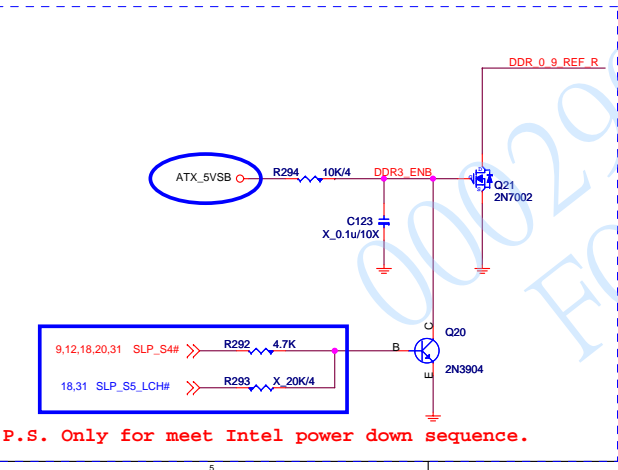
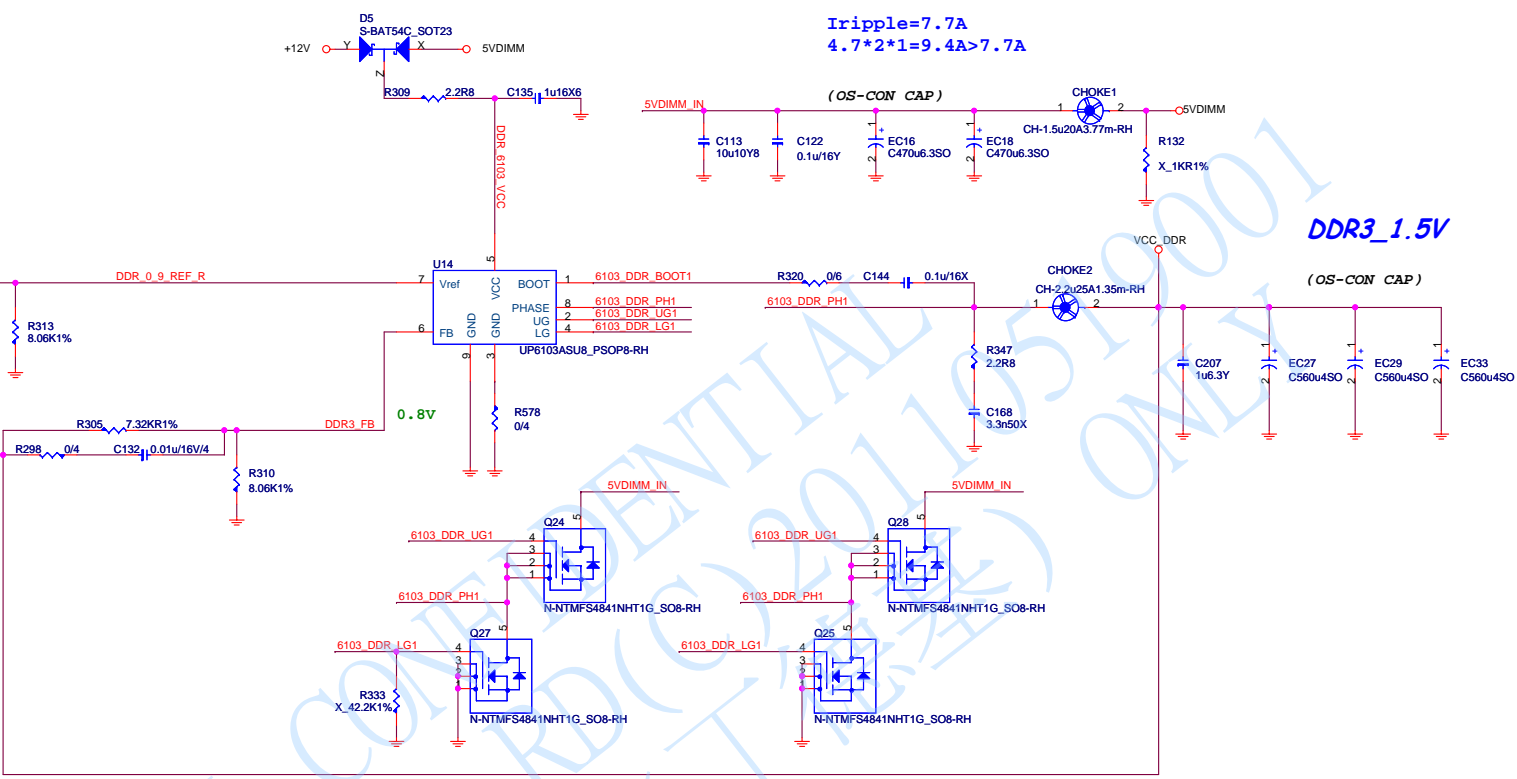
DDR3\_1.5V 4.5A+15A+1A=20.5A

4.5A FOR CPU  
15A FOR 4DIMM  
1A FOR DDR VTT

SIO 出來是 0.9VREF

18 DDR\_REF >> R308 1K/1% C140 0.1u/25Y R313 8.06K1% DDR\_0.9\_REF\_R

0.9V\*8.06K / (1K+8.06K) = 0.795V  
0.795V (1+ 7.15K/8.06K) = 1.5V (VCC\_DDR)



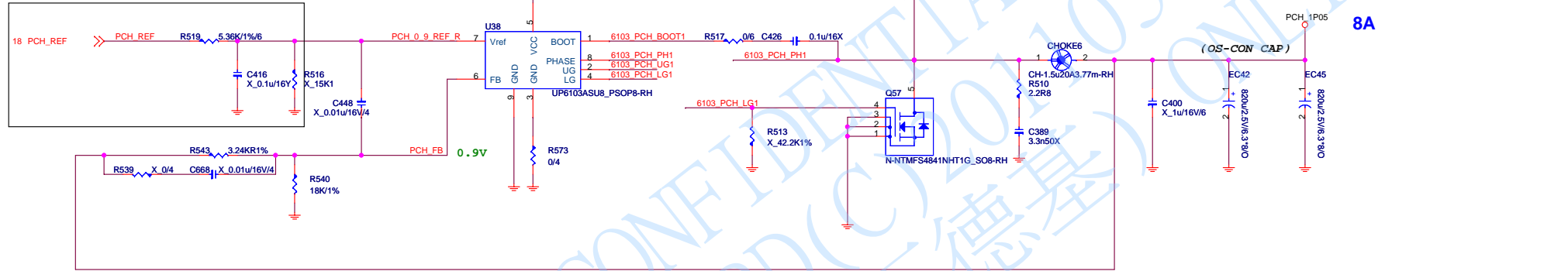
MICRO-STAR INT'L CO.,LTD			
MS-7676			
Size	Document Description	Rev	
Custom	DDR Power - uP6103 1-Phase	2.1	
Date:	Friday, May 13, 2011	Sheet	33 of 47



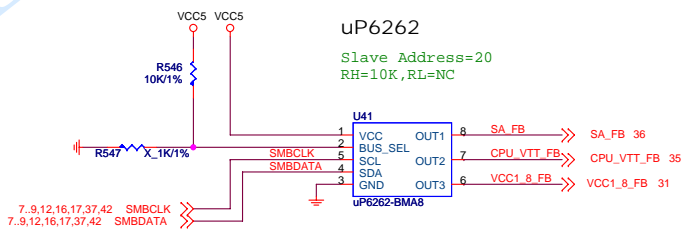
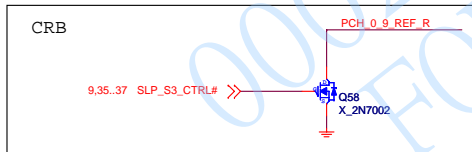
PCH Power:1.05V  
PCH Core 6.2A+1.8A=8A  
6.2A FOR PCH  
1.8A FOR ME CORE

SIO 出來是 0.9VREF

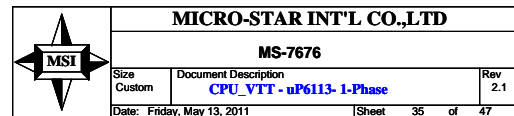
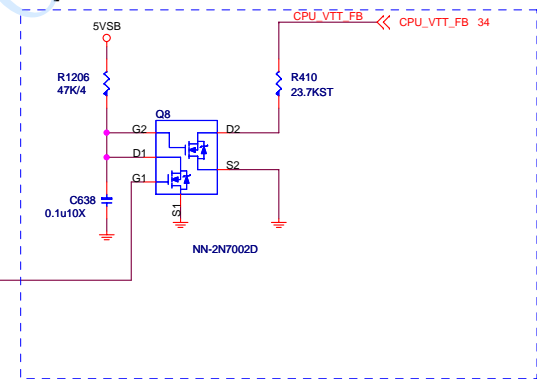
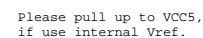
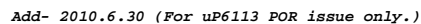
FOR SIO REF



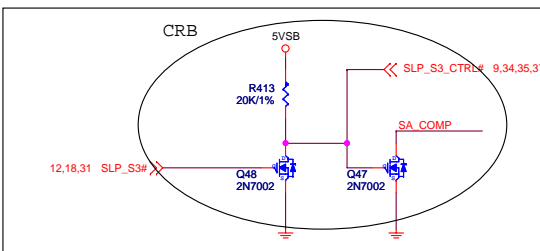
UPI VOLTAGE CONSOLE

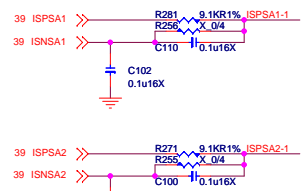
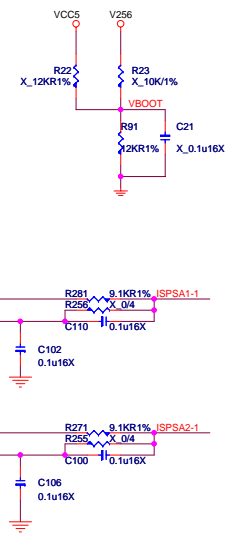
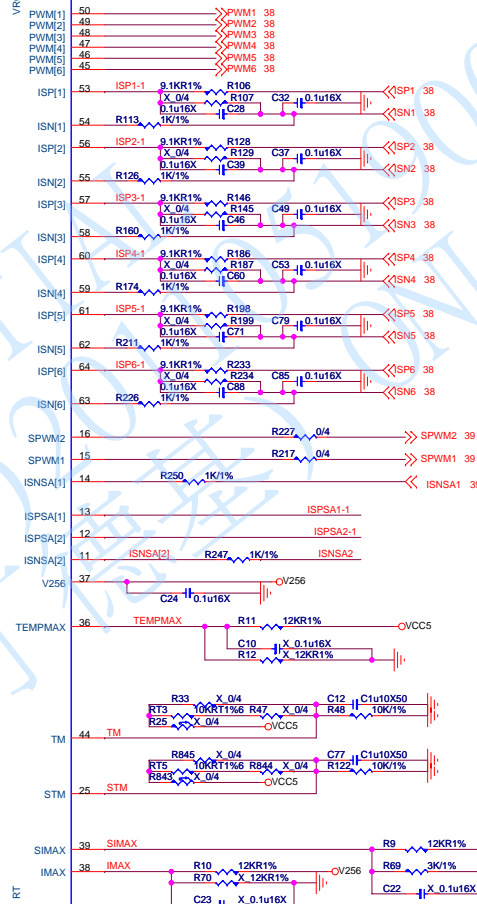
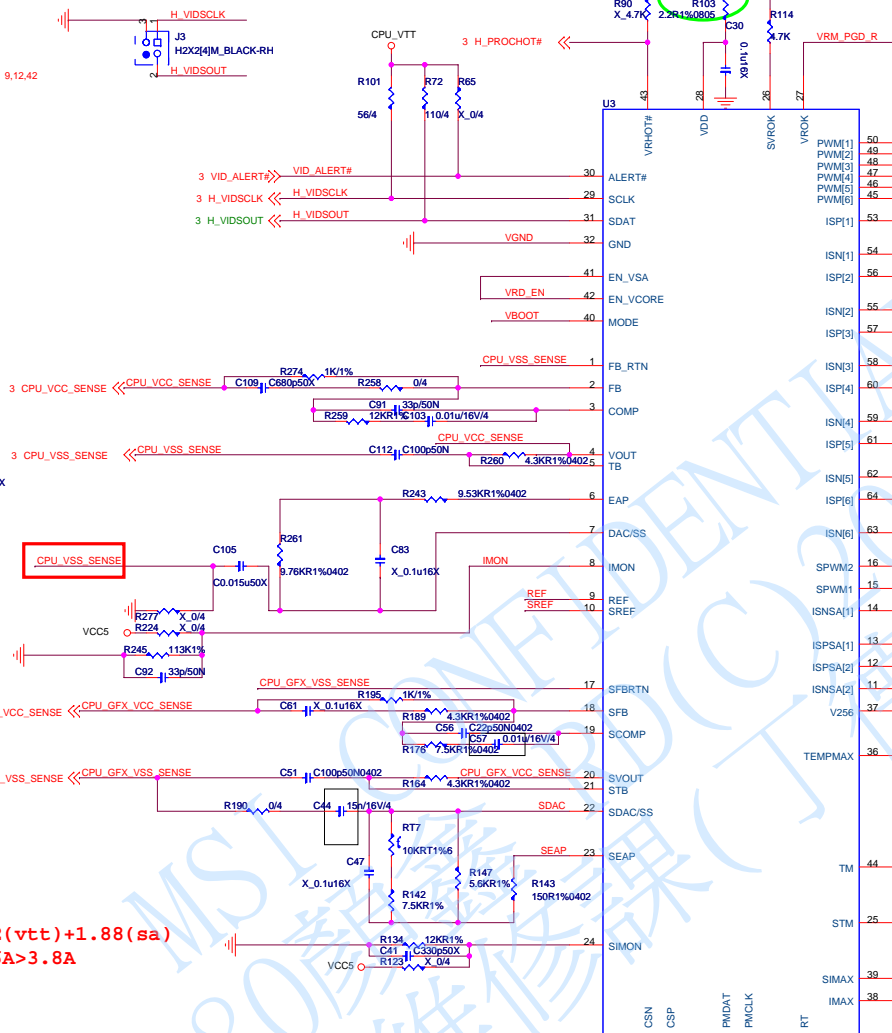
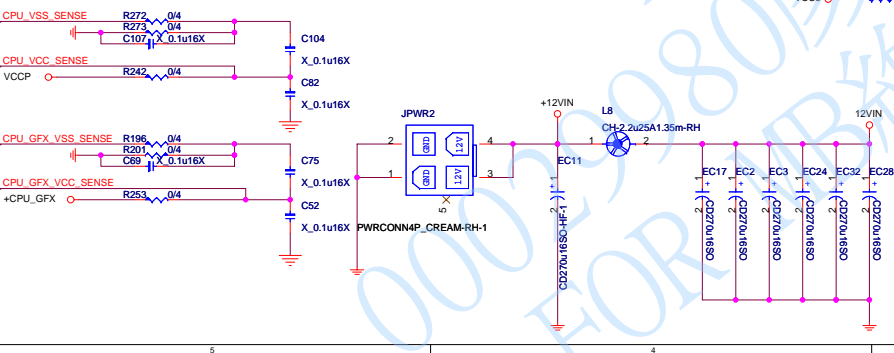
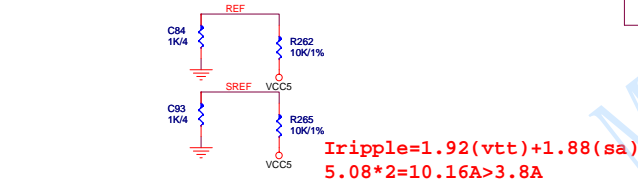
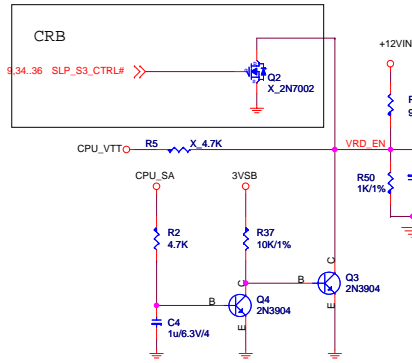


MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size	Document Description	Rev
Custom	PCH Power - uP6103 1-Phase	2.1
Date:	Friday, May 13, 2011	Sheet 34 of 47



**SA Core = 8.8A**

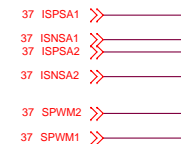




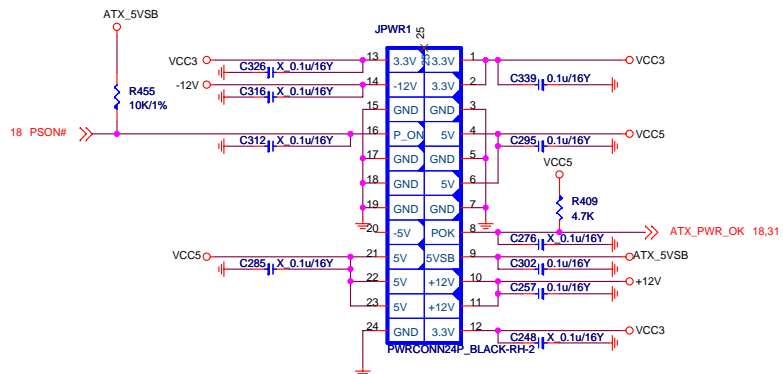
Size Custom	Document Description <b>VRD12 - UPI6234 6+2-Phase</b>	Rev 2.1
Date: Friday, May 13, 2011	Sheet 37 of 47	



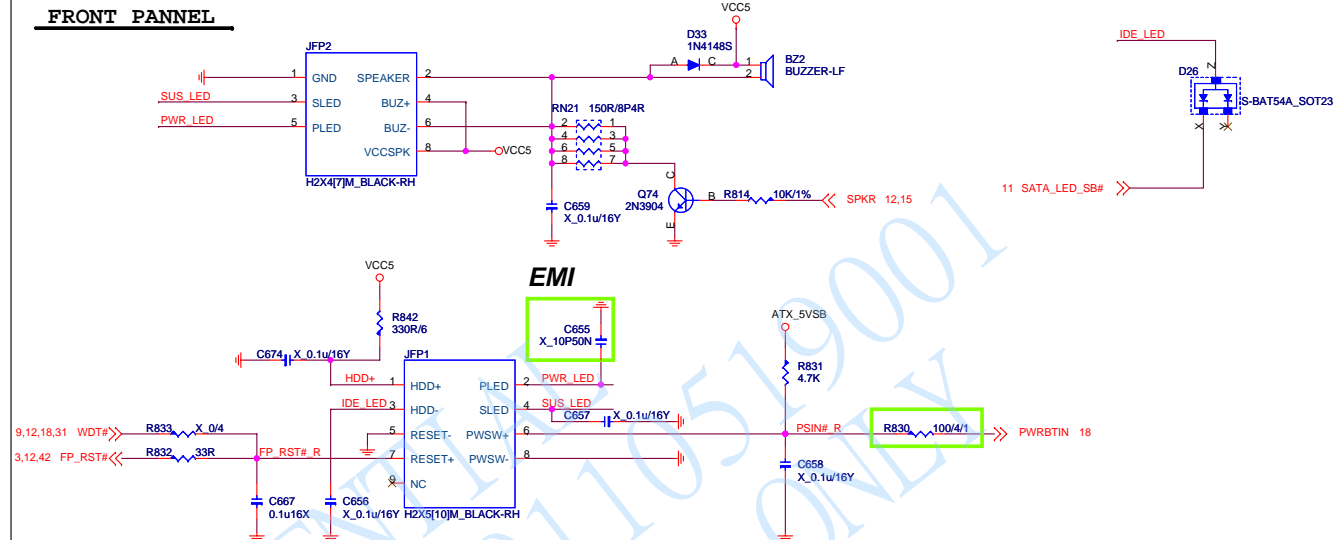




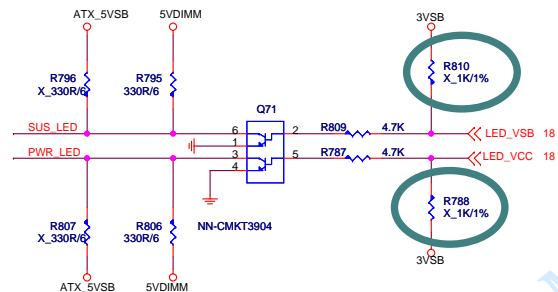
## ATX POWER CONNECTOR



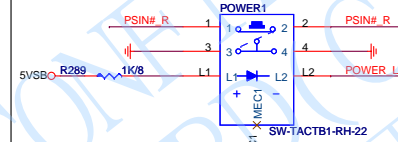
## FRONT PANNEL



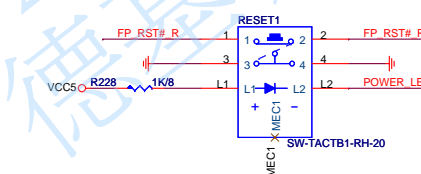
## LED ( for Fintek 71889)



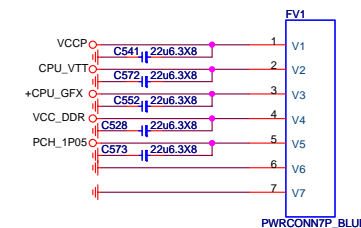
## POWER ON BUTTON



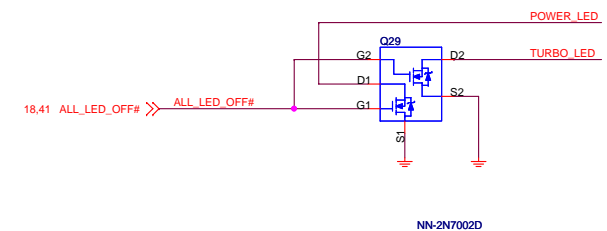
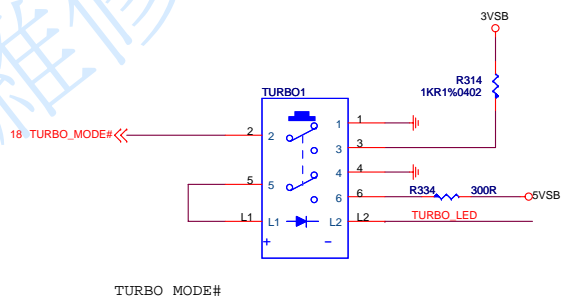
## RESET BUTTON



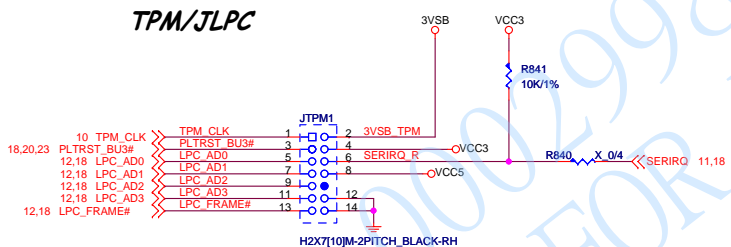
## 電壓測點



## DPS Turbo Button

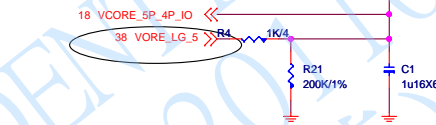
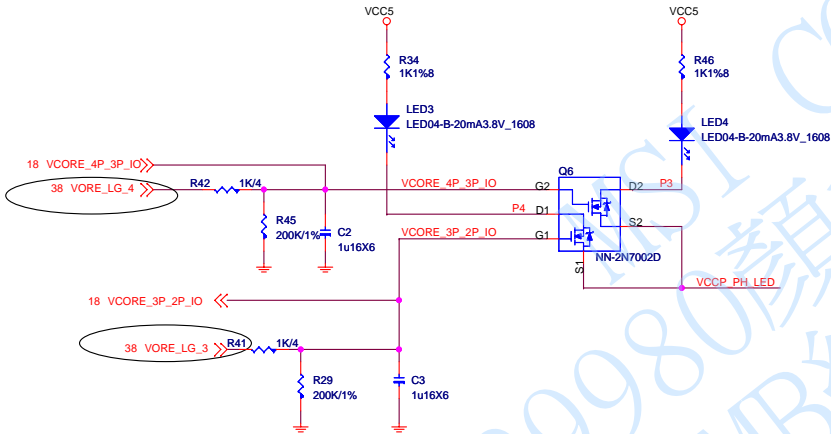
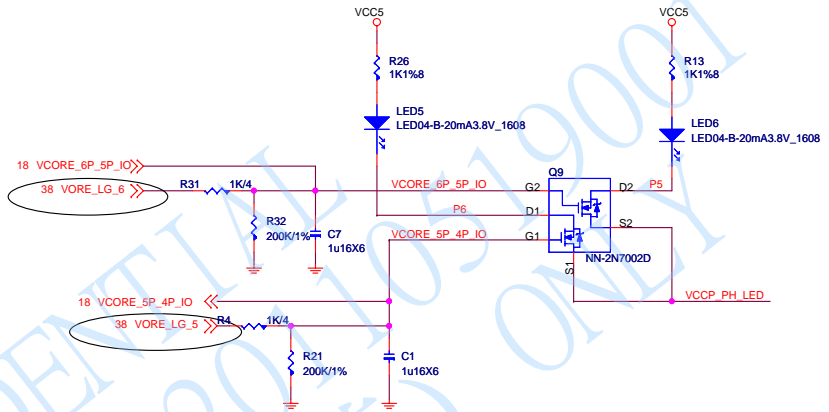
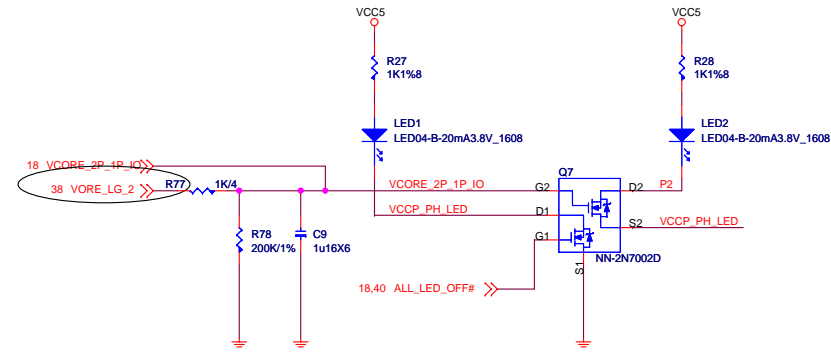


## TPM/JLPC



MICRO-STAR INT'L CO.,LTD			
MS-7676			
Size	Document Description	Rev	
Custom	ATX PWR-Connector & Front Panel & EMI	2.1	
Date:	Friday, May 13, 2011	Sheet	40 of 47

all on board LED switch

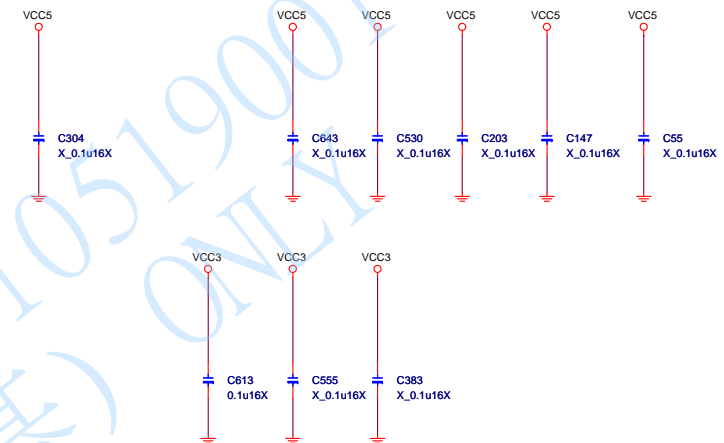


MICRO-STAR INT'L CO.,LTD

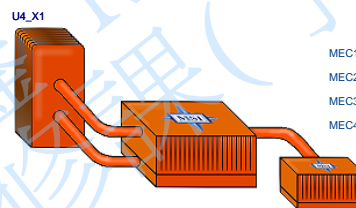
MS-7676

Size	Document Description	Rev
Custom	PHASE Dropping & PSI & LED	2.1
Date: Friday, May 13, 2011	Sheet 41 of 47	

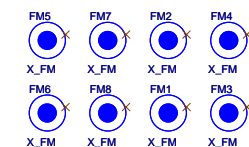
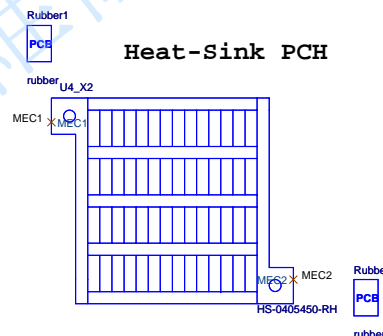
### PCH XDP



## CRB 0.7 107 page



Heat-Sink PCH



MS-7676

Size Custom	Document Description <b>XDP / Manual Parts</b>	Rev 2.1
Date: Friday, May 13, 2011		Sheet 42 of 47